6 - Baseband Description and Troubleshooting

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Abbreviations

ACI	Accessory Interface
APE	Application Processor Engine
ASIC	Application Specific Integrated Circuit
BB	Baseband
BT	Bluetooth (Low range radio link standard)
CCS	Customer Care Solution
CMT	Cellular Mobile Telephone
CSR	Cambridge Silicon Radio
DAC	Digital to Analog Converter
DC/DC	Switched mode power supply
DCT4.x	Digital Core Technology, fourth.x generation
DSP	Digital Signal Processing
EEPROM	Electrically Erasable Programmable Read Only Memory
EM	Energy Management
EMC	Electro Magnetic Compatibility
EMIFF	External Memory Interface Fast
EMIFS	External Memory Interface Slow
ESD	Electro Static Discharge
FBUS	Serial bus
FM	Frequency Modulation
GSM	Global System for Mobile communications
HSCSD	High Speed Circuit Switched Data
HW	Hardware
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
IO	Input / Output
JTAG	Joint Test Action Group – a standard trace and debugging interface
LDO	Low Drop Out
MBUS	Serial bus

MCU	MicroController Unit
MMC	Multi-Media Card
NAND	Flash memory cell type
OMAP	Open Multimedia Architecture Platform
OSP	Organic Solderable Preservative
PA	Power Amplifier
PWB	Printed Wiring Board (same than PCB)
RF	Radio Frequency
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SPR	Standard Product Requirements
SW	SoftWare
UEM	Universal Energy Management Asic (DCT4 EM asic)
UI	User Interface
UPP	Universal Phone Processor ASIC (DCT4 processor asic)
USB	Universal Serial Bus
WLAN	Wireless LAN

Baseband Top-Level Description

RA-2/3 HW is based on a platform with a WLAN subsystem.

RA-2/3 HW architecture consists of:

- Two colour displays
- QWERTY keyboard
- Cover keyboard
- Engine PWB

There are three PWBs: main engine board, QWERTY PWB and lid flex. Both displays and the cover keyboard are connected to the engine via the lid flex. The QWERTY keyboard is connected to the engine through a QWERTY controller. Camera is located directly on the engine PWB.

RA-2/3 engine PWB architecture consists of four main building blocks:

- Application Processor Engine (APE)
- Cellular Mobile Telephone (CMT)
- WLAN and
- CMT RF

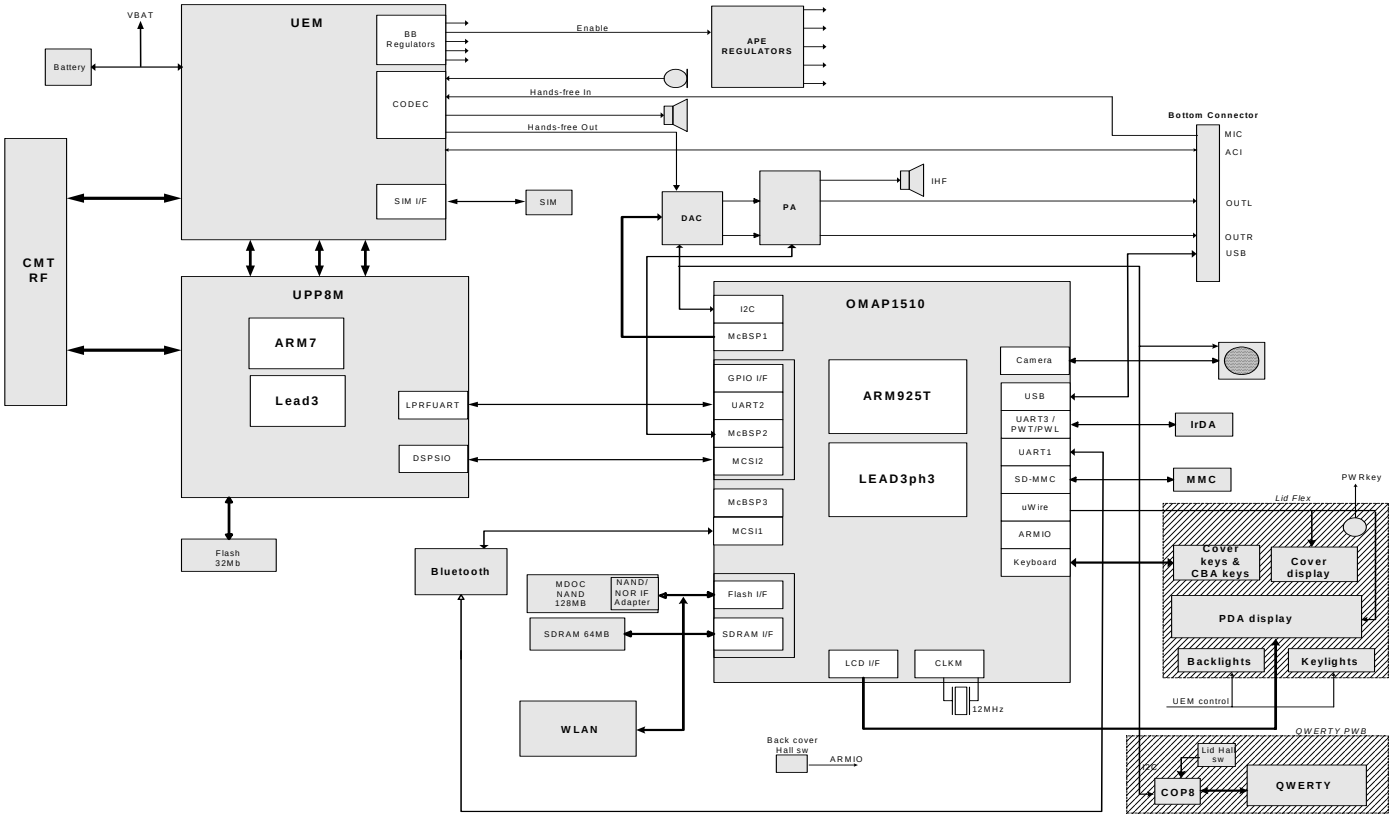
The APE part is constructed using OMAP1510 processor with external SDRAM and NAND based flash memory as the core. Other major parts for APE are power supplies, UI interfaces, audio support, Bluetooth and camera.

The WLAN subsystem is connected to the OMAP1510 flash interface. WLAN baseband is based on T TNETW1100B Medium Access Controller / Baseband Processor IC. The 2.4GHz radio part is based on zero-IF transceiver and PA. Bluetooth and WLAN share the same antenna and cannot be active simultaneously.

APE and CMT parts are connected together by serial communication buses and by a few control lines. The APE part reset and power control comes from the CMT side. Audio control is mostly on the APE side. APE and CMT operate with no clear master-slave nomination.

The diagram below shows a high level block diagram of RA-2/3.

Figure 1:Simplified RA-2/3 block diagram



Operating conditions

Absolute maximum ratings

Table 1: Absolute maximum ratings

Signal	Note
Battery Voltage (Idle)	-0.3V - 5.5V
Battery Voltage (Call)	Max 4.8V
Charger Input Voltage	-0.3V - 16V

Battery voltage maximum values are specified during active charging.

DC characteristics

Table 2: Battery voltage range

Signal	Min	Nom	Max	Note
VBAT	3.1V	3.6V	4.2V (charging high limit voltage)	3.4V SW RF cut off

Battery maximum voltage is specified when charging switch is disconnected after/between charging pulses.

Temperature conditions

Full functionality is achieved in the ambient temperature range -15 ^{o}C to +55 ^{o}C. Reduced functionality between -25 ^{o}C to -10 ^{o}C and +55 ^{o}C to +70 ^{o}C.

The required storage temperature is -40 ^{o}C to +85 ^{o}C.

ESD immunity

SPR limits are 8kV for galvanic contact and 15kV for air discharge with normal and reversed polarity.

Functional Description of CMT

The CMT architecture of RA-2/3 is based on DCT4 Common Baseband. The main functionality of the CMT baseband is implemented into two ASICs: UPP (Universal Phone Processor) and UEM (Universal Energy Management).

32Mbit NOR flash is used to store the program code. For a simplified block diagram of the RA-2/3 CMT baseband, see Figure 2, “Simplified CMT baseband block diagram” on page 11.

System clock for the CMT is derived from the RF circuits. For GSM it is 26 MHz. The low frequency sleep clock is generated in the UEM using an external 32.768 kHz crystal. The I/O voltage of the CMT baseband is 1.8V and the analog parts are powered from 2.8V power rails. The core voltage of UPP can be altered with SW depending on the prevailing processing power requirements.

UEM is a dual voltage circuit. The digital parts are running from the baseband supply (1.8V) and the analog parts are running from the analog supply (2.8V). Some blocks of UEM are also connected directly to the battery voltage (VBAT). UEM includes 6 linear LDO (low drop-out) regulator for the baseband and 7 regulators for the RF. It also includes 4 current sources for biasing purposes and internal usage.

Some parts of the SIM interface have been integrated into UEM. The SIM interface supports only 1.8V and 3V SIM cards. Data transmission between the UEM and UPP is handled via two serial buses: DBUS for DSP and CBUS for MCU. There are also separate signals for PDM coded audio. Digital speech processing is handled by the DSP inside UPP and the audio codec is in UEM.

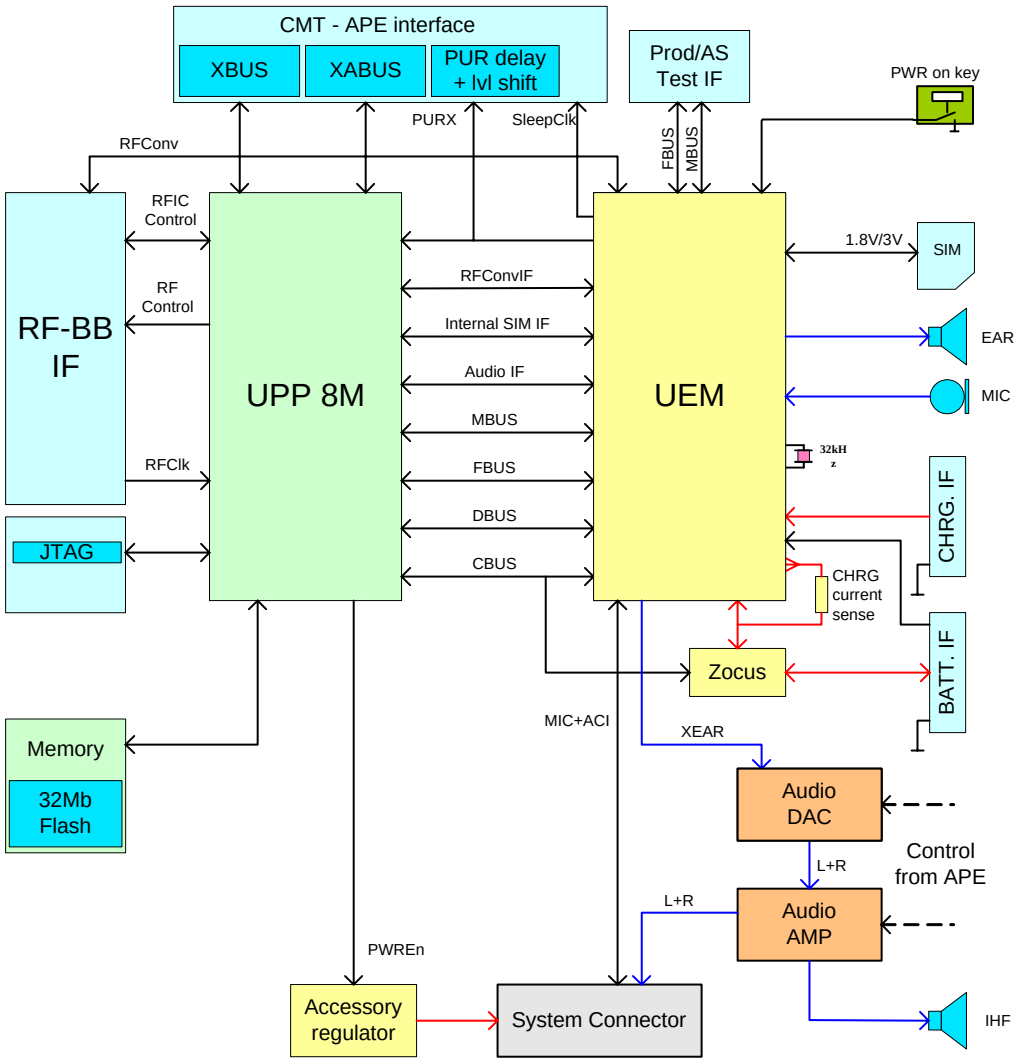
The analog interface between the baseband and the RF sections has been implemented into UEM. UEM provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and supplies the analog TXC and AFC signals to RF section under the UPP DSP control. The digital RF-BB interface, consisting of a dedicated RFIC control bus and a group of GenIO pins, is located in the UPP.

The baseband side supports both internal and external microphone inputs and speaker outputs. Input and output signal source selection and gain control is performed in the UEM according to control messages from the UPP. Keypad tones, DTMF, and other audio tones are generated and encoded by the UPP and transmitted to UEM for decoding.

RA-2/3 has two galvanic serial control interfaces for CMT: FBUS and MBUS.

Communication between the APE and CMT parts is handled through 2 serial buses: XBUS and XABUS. XBUS is the main communication channel for general use, and XABUS is intended mainly for audio data transfer. Also the system reset (PURX) and SleepClk for APE are taken from the CMT side. The PURX is delayed approximately 130ms to fulfil OMAP1510 reset timing requirements. One of UEM’s IR level shifters is used for SleepClk level shifting both to APE and WLAN.

Figure 2:Simplified CMT baseband block diagram



Interfaces between CMT and APE

XBUS

XBUS is the main communication interface between the CMT and APE parts of RA-2/3. This 6-pin interface is implemented using UART2 of OMAP1510 (APE), LPRFUART of UPP (CMT) and 2 general purpose I/O pins from both ASICs.

XABUS

XABUS is a synchronous serial interface which is used for uncompressed PCM audio data transfer between the DSPs of UPP (CMT) and OMAP1510 (APE). This interface utilises the DSPSIO of UPP and the MCSI_2 of OMAP1510. In addition to these one UPP GenIO and two dedicated pins of OMAP1510 are needed for XABUS clock generation and control.

Functional Description of APE

APE term includes not only the processor itself but also the peripherals around it, clocking, re-setting and power management for these parts.

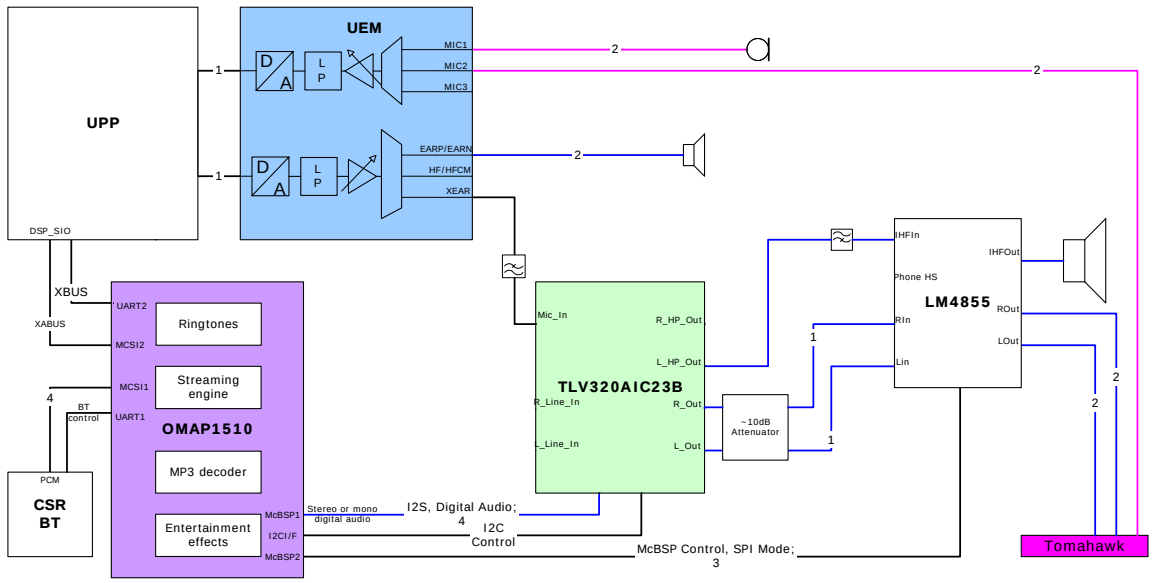
APE is based around OMAP1510 (Open Multimedia Application Platform) processor. Peripherals attached to OMAP1510 include:

- Audio DAC
- Camera
- Bluetooth
- Cover display
- PDA display
- Memory card
- IrDA
- Cover keypad & CBA buttons
- QWERTY controller
- External SDRAM
- Flash memories
- WLAN

APE acts as a system slave compared to the CMT side. CMT holds the master reset and power management logic. APE and CMT are connected through a serial link called XBUS.

Audio

Figure 3:RA-2/3 Audio architecture



As RA-2/3 is based on a dual-processor architecture, audios are also divided into APE and CMT parts. Audio control is mostly on the APE side. Phone audio is routed from the CMT side

to APE in analog form. On the CMT side, audio HW is integrated into the UEM ASIC. On the APE side, the most important parts are OMAP1510, audio DAC and audio power amplifier.

The stereo output of this amplifier is designed for use with the extended Pop-port^{TM} connector. It also has a differential mono output for driving the handsfree speaker.

The battery voltage (VBAT) is used directly as a supply voltage for the audio amplifier.

The type of DAC used is TLV320AIC23B and the supply voltage for this is coming from V28.

Audio control signals

Audio DAC is controlled via I^{2}C bus by OMAP1510. Digital audio data from OMAP1510 to DAC is coming via MCBSP1.

The audio amplifier is controlled through a 3-wire SPI bus (MCBSP2 of OMAP1510). Audio mode of the amplifier and gain values are controlled via SPI bus.

The HEADINT signal is needed for recognising the external device (e.g. headset) connected to system. The recognition is based on the ACI-pin of the system connector, which is shorted to ground inside the external device.

The button of the external device generates HOOKINT interrupt and is used to answer or end a phone call.

Audio modes

HP call

The basic audio mode is the hand portable mode. This is entered when no audio accessories are connected and handsfree mode is not selected by opening the cover.

The call is created by CMT. The internal earpiece is driven by the CMT engine for voice calls. The internal microphone is driven by the CMT for voice calls and voice recording. The internal microphone is enabled and uses the MICB1 bias voltage from UEM.

IHF call

This mode can be entered by user selection (opening the cover).

The call is created by CMT. The internal microphone is driven by the CMT for voice calls and voice recording. The internal microphone is enabled and uses the MICB1 bias voltage from UEM as in HP mode.

XEAR output of UEM is used to drive mono output signal is connected to the APE Audio DAC. Signal is then routed to the Phone_In_IHF input of the LM4855. This drives the internal speaker via the SPKRout driver.

Accessory call

This mode is used when accessory is connected to the system connector.

The call is created by CMT. The uplink signal is generated by external microphone and transferred to UEM MIC2 input (via XMIC signals from Pop-port^{TM} connector). Hence the MIC2B bias voltage and MIC2P/N inputs are enabled on UEM.

As in IHF call down link audio signal is routed through the single ended XEAR output driver in UEM. The mono XEAR output is connected to the DAC and then signal is routed to the L_{IN} and

R_{IN} inputs of the LM4855. Accessories are driven via Pop-port™ connector using the L_{OUT} driver of LM4855.

APE audio

This mode is entered when user starts the multimedia application (e.g. MP3, AAC etc.), which is played via IHF speaker or Pop-port™ accessories.

Audio data from MMC is sent by OMAP1510 to the external audio DAC through the I^2S connection. The DAC performs the digital to analog audio conversion.

For playback via the internal speaker signal from DAC is routed to Phone_in_IHF input on LM4855.

For playback via the stereo/ mono headset or other Pop-port™ accessories signal from DAC is routed to the L_{IN} /R_{IN} inputs of the LM4855. In case of mono accessory OMAP1510 will produce monophonic signal to DAC.

Internal interfaces

In practice, all APE internal interfaces consist of interfaces connected from OMAP1510 to peripheral devices. All UI related interfaces, memory interfaces, USB and MMC are covered in separate sections of this document.

McBSP interfaces

OMAP1510 can support maximum of three independent Multi-channel Buffer Serial Ports (McBSPs) interfaces. However, these ports are slightly different and particularly suitable for different purposes. McBSP1 supports I2S protocol and is connected to external audio codec. McBSP#2 and #3 can be used as general purpose SPI interface supporting bit rates up to 5Mbits/s. McBSP2 is used to control the audio PA. McBSP3 clock output is used as audio codec master clock. Other McBSP3 signals cannot be used because they are multiplexed with uWire signals.

MCSI interfaces

The MCSI is a serial interface with multi-channels transmission capability. MCSI1 is used to interface with Bluetooth and MCSI2 is used as XABUS (DSP-DSP bus between CMT and APE)

UART interfaces

OMAP1510 has three UART interfaces capable of 1.5Mbit/s data rates. UART1 is used as Bluetooth control interface, UART2 is used as XBUS (MCU-MCU bus between CMT and APE), UART3 includes 115.2 kbit/s IrDA modulation support, and is used to communicate with external IrDA device.

UWire interface

The uWire interface is a standard serial synchronous bus protocol with two chip select lines. Interface is used as PDA LCD control bus (CS3) and as a unidirectional data bus for the Cover display (CS0).

I2C

The I^2C is a half-duplex serial port using two lines, data and clock, for data communications with software addressable external devices. I^2C is used as audio codec and camera module control bus. External keyboard controller COP8 is also connected to APE via I^2C.

ARMIO

ARMIO provides 5 ARM processor controllable GPIOs by default, and 5 more are available with different multiplexing scheme. ARMIOs also include a keyboard interface. The GPIOs consists programmable debouncing circuit but can be accessed directly only by the ARM processor. Both ARMIOs and keyboard interface signals can wake-up OMAP1510 from deep sleep and big sleep states.

GPIO

14 General Purpose Input/ Output External pins are multiplexed between ARM/DSP. Multiplex logic is programmed and controlled by ARM and supports pin-by-pin configuration.

External interfaces

Back cover switch

A hall switch is used for back cover removal detection. A magnet is attached to the back cover. A sensor gives a warning to prevent data loss or corruption when writing to the MMC card.

Lid hall switch

A hall switch is used to detect the lid position. The switch is located on QWERTY PWB and is connected to COP8 controller. The magnet is in the lid.

MMC

The MMC Interface in OMAP1510 is fully compliant with the MultiMediaCard system specification version 3.1. RA-2/3 MMC interface voltage is 3 V.

USB

The OMAP1510 USB Controller is a Full Speed Device (12 Mb/s) fully compliant with the Universal Serial Bus specification Revision 2.0. The USB Client (a mobile terminal) is connected to the USB Host (a PC) through the system connector.

UI interfaces

Displays

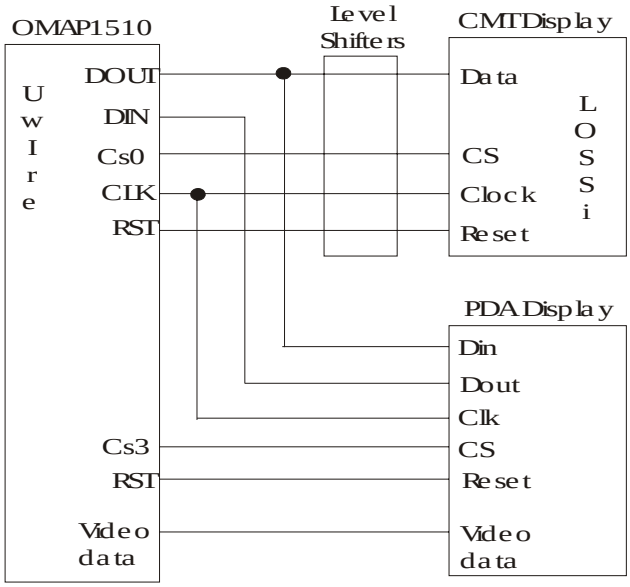
S80 display interface

S80 display utilizes the 16-bit synchronous LCD interface of OMAP1510, and uWire for control data.

Cover display interface

RA-2/3 has a separate small 65k colours display connected to OMAP1510 via uWire interface. There is an unidirectional level shifter between OMAP and the display, so no data can be read from the display.

Figure 4:Display interfaces



Keyboards

Cover keyboard and CBA buttons

The cover keyboard and the four CBA buttons are directly connected to the OMAP1510 keyboard matrix.

QWERTY

An external keyboard controller is used for the QWERTY keyboard. COP8 is connected via I2C bus to OMAP1510 with an additional interrupt line to OMAP1510.

Power button

The power button is connected directly to UEM in the DCT4 engine. See Chapter Power up and system states for further details on the power button operation.

Camera

8-bit parallel camera interface connects OMAP1510 chip to the camera module. I2C bus is used for controlling the camera module.

Main features

Imaging and resolution:

- VGA resolution 640x480
- 1/4" sensor area
- 16bit colours (5+6+5 / R+G+B)
- Frame rate 15fps in all modes (30fps for QVGA, QQVGA, QCIF and subQCIF)
- Three different exposure modes: normal, long (frame rate / 4) and extra long mode.

- Automatic image features: luminance level control, white balance control, blemish detection and control, fluorescent flicker frequency detection

Optics:

- Fixed focus (from 30cm to infinity)
- Two plastic lenses with antireflection coating
- Viewing angle 50.7 degrees
- F 2.8

Interface

The camera module contains a CMOS image sensor, image processing functions, camera image data IF (8-bit parallel data interface + sync and clock signals) and control IF blocks. The camera is connected to the camera interface of the OMAP1510. I2C interface is used for camera control (slave address 78H). Control IF supports transfer rate up to 400kbit/s (Fast mode I2C bus). Parallel image data stream is conformity with CCIR656. OMAP1510 contains camera interface block, which contains the buffer, the clock divider, the interrupt generator, and Rhea registers.

The camera module is connected to OMAP1510 processor on Nokia engine PWB via flex and a 20-pin connector. Description and order of the signals are shown in Table 3, “Interface signals of camera module with 20-pin connector”. All the signals go through the camera flex.

Table 3: Interface signals of camera module with 20-pin connector

Pin #	Signal name (Camera)	Signal name (Engine)	I/O/Z	Description
1	GND1	GND	-	Ground line corresponding to VDDI
2	D0	CAM_D0	O	Digital output data (LSB)
3	SDA	SDA	I/O	Serial data line of I^2C bus
4	D1	CAM_D1	O	Digital output data
5	SCL	SCL	O	Serial clock line of I^2C bus
6	D2	CAM_D2	O	Digital output data
7	VDDI	V18	-	Supply voltage to a camera module (for digital)
8	D3	CAM_D3	O	Digital output data
9	Extclk	CAM_EXCLK	I	System clock from Nokia engine to the camera module. Typical value for camera is 1.0 V.
10	D4	CAM_D4	O	Digital output data
11	GND3	GND	-	Ground line corresponding to Extclk
12	D5	CAM_D5	O	Digital output data
13	HD	CAM_HS	O	Horizontal synchronization data
14	D6	CAM_D6	O	Digital output data
15	VD	CAM_VS	O	Vertical synchronization data
16	D7	CAM_D7	O	Digital output data (MSB)
17	VDD	V28	-	Supply voltage to camera module (for analog and I/O)
18	Dclk	CAM_LCLK	O	Data clock synchronization pulse
19	Vctrl	CAM_RSTZ	I	Activating signal for the camera module (active HIGH). The min. high level of Vctrl must be 1.5 V. Voltage divider used.
20	GND2	GND	-	Ground line corresponding to VDD

Bluetooth

A single chip Bluetooth solution, BC02, is used in RA-2/3. The chip contains radio and baseband parts as well as MCU and on-chip ROM memory. Together with some external components (filter, balun etc.) and the antenna, it forms the Bluetooth system, which is attached to the host (OMAP1510). Bluetooth components are mounted directly to the PWB. Bluetooth antenna and filter are shared with WLAN.

IrDA

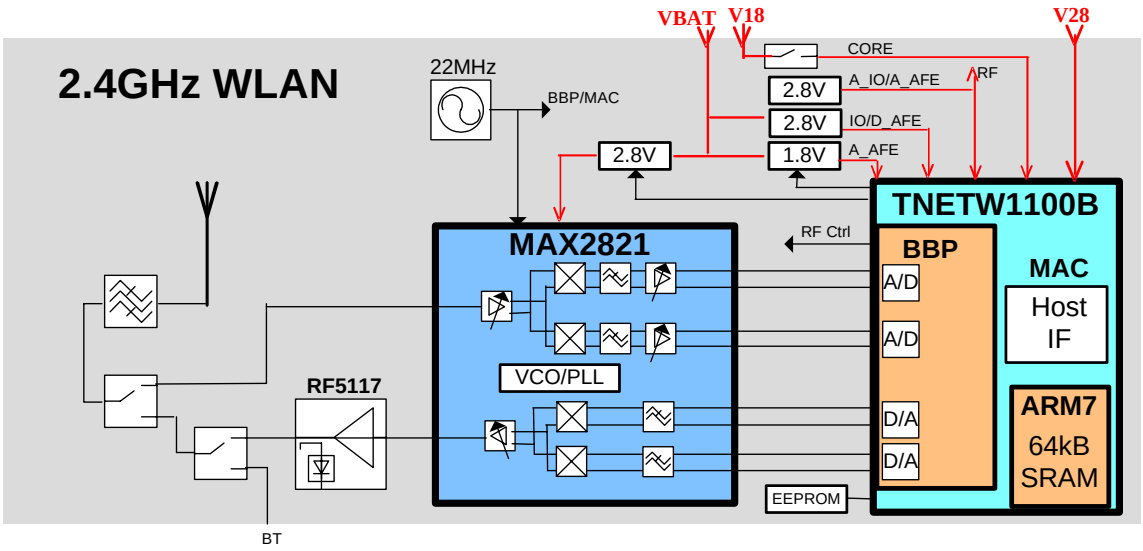
RA-2/3 design includes a small (height 2.2 mm) metal shielded module. The modules use speeds up to 115.2kbps.

Functional Description of WLAN

RA-2/3 has an integrated 11Mbps 802.11b capable WLAN radio. WLAN power supply is based on a set of linear regulators and a load switch. A 22MHz crystal oscillator supplies main WLAN clock. Bluetooth shares the same physical antenna with WLAN.

The TNETW1100B MAC/BPP is connected to OMAP1510 flash memory interface via 16 data bits and 4 address bits, plus some control lines.

Figure 5:RA-2/3 WLAN block diagram



WLAN medium access controller

TNETW1100B implements basic IEEE802.11 functionality. The system is built on Arm7 and a dedicated DMA controller. Dedicated hardware accelerators for MAC protocol processing and WEP offload the processor. The chip integrates SRAM for storing both data and code.

DMA controller connects data memory and host interface with processor and baseband processor interface. Transmit and receive data buffers are implemented as linked lists of memory blocks. The DMA engine is capable of handling the lists without intervention from embedded Arm.

Clocking, reset and wake-up

WLAN uses a 22 MHz reference clock CMOS level signal. The reference oscillator has logic level enable signal and low-power sleep mode. The reference oscillator is controlled by a TNETW chip.

The sleep clock is derived from the GSM engine and it is constantly running. UEM generates 32 kHz sleep clock at 1.8 V signal level. UEM internal level converter is used to raise the sleep clock level to 2.8 V. The same sleep clock is used for both Helen and TNETW.

A Helen GPIO controls TNETW reset. Another GPIO controls the main power supplies to the WLAN hardware.

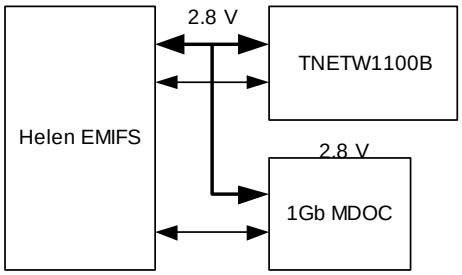
Power up sequence

1. Helen enables the WLAN power regulators with a GPIO.
2. 50 ms delay to enable the WLAN powers to stabilize.
3. Helen takes the WLAN out of reset with a GPIO.
4. Helen configures EMIF_CS.
5. Helen activates TNETW1100B interface delay logic and enables the enhanced slave mode.
6. Helen checks if the EEPROM is empty, and if it is empty, Helen programs a default content to it.
7. Helen downloads the WLAN firmware to the TNETW1100B and initializes it.
8. Power up sequence is complete.

WLAN – OMAP host interface

TNETW1100B is connected to Helen external memory interface (EMIFS). The interface is shared with RA-2/3 flash system consisting of NAND flash + controller on the same die (MDOC).

Figure 6:TNETW1100B and NAND Flash share Helen EMIFS interface



TNETW1100B host interface I/O voltage is 2.8 V. Therefore the MDOC host interface also runs at 2.8V

Two GPIOs from Helen are used for controlling the WLAN hardware. One GPIO controls the main power supply regulators for WLAN, and the other is used for resetting the TNETW. One Helen Armio is used to generate interrupt from WLAN when Helen is in sleep. Helen can go to deep sleep while WLAN is active, ARMIO is capable of waking it up.

WLAN baseband processor

Baseband processor part of TNETW1100B implements signal processing required for transmission and reception of the IEEE802.11b signal. BBP includes mixed-signal interface to the radio (analog front-end, AFE).

Receiver portion of BBP controls the radio receive AGC and DC offset compensation circuitry. The receiver is capable of processing both long and short preambles and supports Barker and CCK modulations as well as proprietary 22 Mb/s PBCC mode.

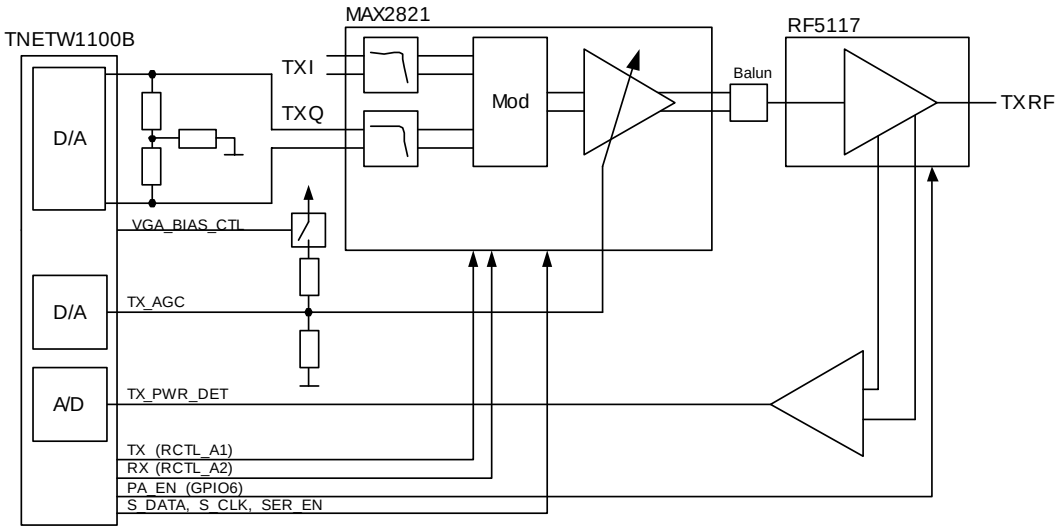
Transmitter RF-BB interface

Transmitter RF-BB interfaces are shown in Figure 7, “Transmitter RF-BB interfaces” . TNETW has on-chip current mode differential output dual DAC for generating transmitted I/Q signals.

The converters are clocked at 44 MHz. Current mode output is converted to differential voltage mode signals by means of resistive bias network (Q signal shown, I signal bias network identical). I/Q signals are fed into Maxim MAX2821 RFIC where they are modulated onto 2.4 GHz carrier.

Power amplifier is RF5117, which requires external OpAmp for transmit power detection, see Transmitter RF-BB interfaces.

Figure 7:Transmitter RF-BB interfaces

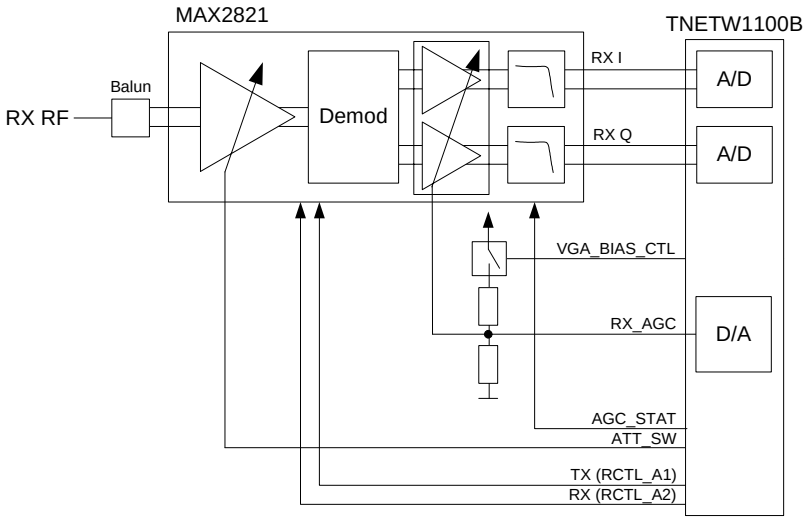


Receiver RF-BB interface

Receiver RF-BB interface is shown in Figure 8, “Receiver RF-BB interfaces” . Incoming RF signal is converted to differential signal in a balun. After balun there is a switchable LNA with high gain and low gain modes. The mode of the LNA is controlled by the TNETW based on the signal level on I/Q ADC output.

RX AGC control signal has a similar switchable resistive bias network as the transmitter chain. The switch is shared with TX AGC bias network.

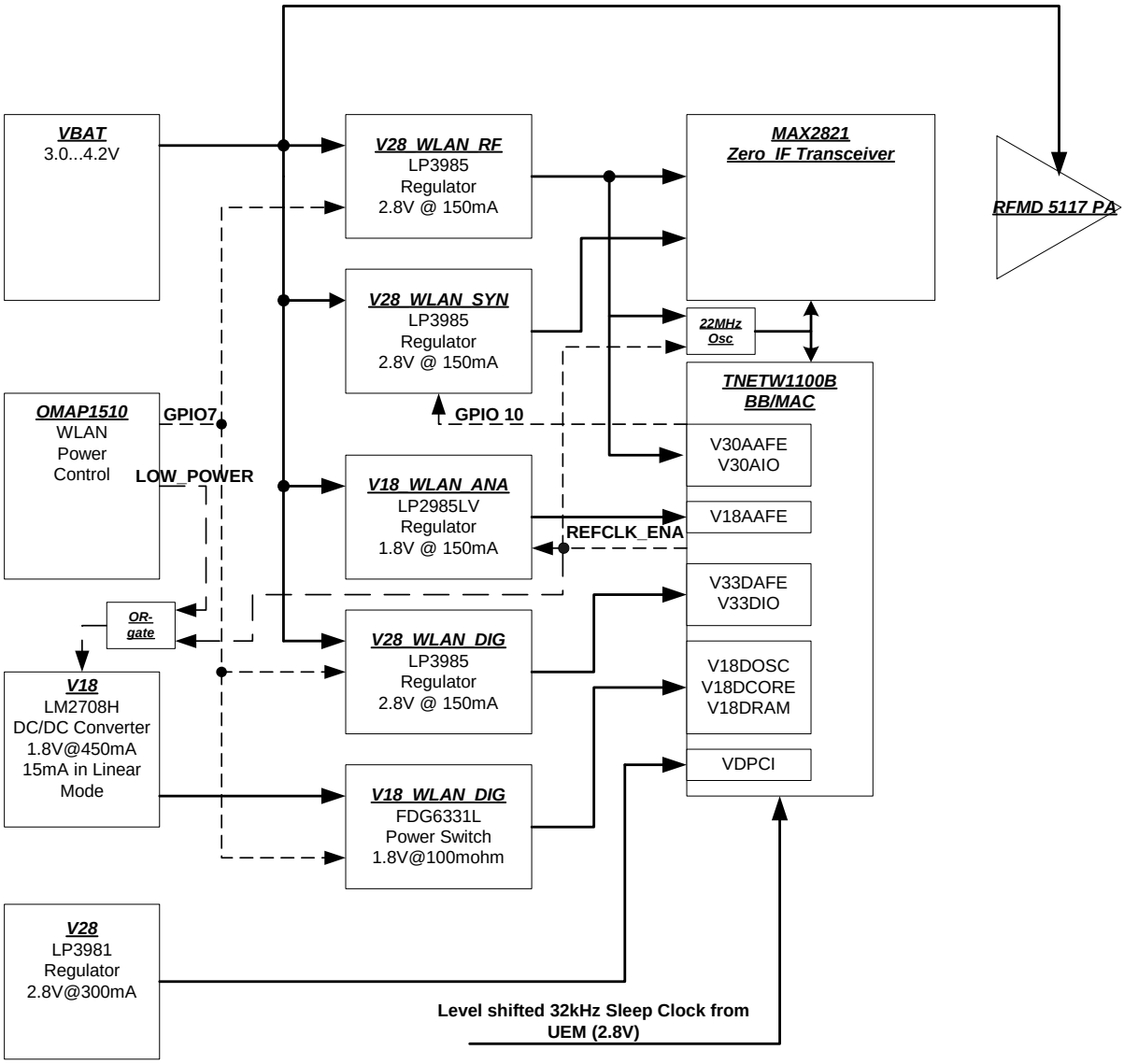
Figure 8:Receiver RF-BB interfaces



WLAN energy management

WLAN regulators

Figure 9:WLAN EM block diagram



The 1.8V voltage for TNETW core and internal RAM is taken from DC-DC converter that is already present for powering Helen, SDRAM, etc. Helen controls the 1.8V voltage to TNETW by a load switch. The same Helen GPIO is used for controlling the 2.8V linear regulator powering WLAN RF, TNETW analog IOs and AFE (analog front end). Another Helen controlled 2.8V linear regulator supplies TNETW digital IOs and D_AFE (digital parts of analog front end).

WLAN controls the DC-DC converter LDO mode together with APE. When WLAN is in active mode (i.e. Not in poweroff, doze or sleep), the REFCLK_ENA signal from TNETW1100B forces the DC-DC converter to active mode.

TNETW controls two regulators to minimize current consumption during sleep mode. The 1.8V regulator supplies the A_AFE (analog parts of analog front end). The 2.8V regulator supplies the synthesizer part of MAX2821.

WLAN RF power amplifier is powered directly from VBAT. VBAT voltage is nominally 3.6 V, but reaches 4.8 V momentarily at the end of the charging. After charging the battery voltage can reach 4.2 V.

The 22 MHz reference oscillator has an enable signal and therefore it has no dedicated regulator.

WLAN EM concept and battery capacity

WLAN engine has two major power management modes: sleep and active. It is also possible to shut down the WLAN for reduced power but the wake-up time is in the order of seconds. Shutting down the WLAN is used when the user chooses to deactivate the WLAN by selecting Bluetooth.

Table 4: WLAN power modes

Mode	Description	Current	Wake-up time
Power Off	WLAN is powered down. Entering active mode requires firmware download and configuration of the WLAN engine. Wake-up can only be initiated by the host.	~ 0 µA	~ 1 s
Deep Sleep	Deep Sleep is physically the same mode as Doze. Logical connection to network is not (yet) established. This is the state after firmware download and issuing sleep command. WLAN runs from 32 kHz sleepclock and 22 MHz reference clock is turned off. Radio is in low current stand-by mode. Analog 1.8V supply to TNETW and 2.8V synthesizer supply are turned off by TNETW to further reduce current consumption.	53µA	2-3 ms
Doze	Doze mode is similar to Deep Sleep mode. Wake-up time is dominated by the 22 MHz reference oscillator start-up time.	53 µA	2-3 ms
Active	In active mode the WLAN system is either in receive or transmit mode.	~220 mA RX, ~270 mA TX. 1)	-

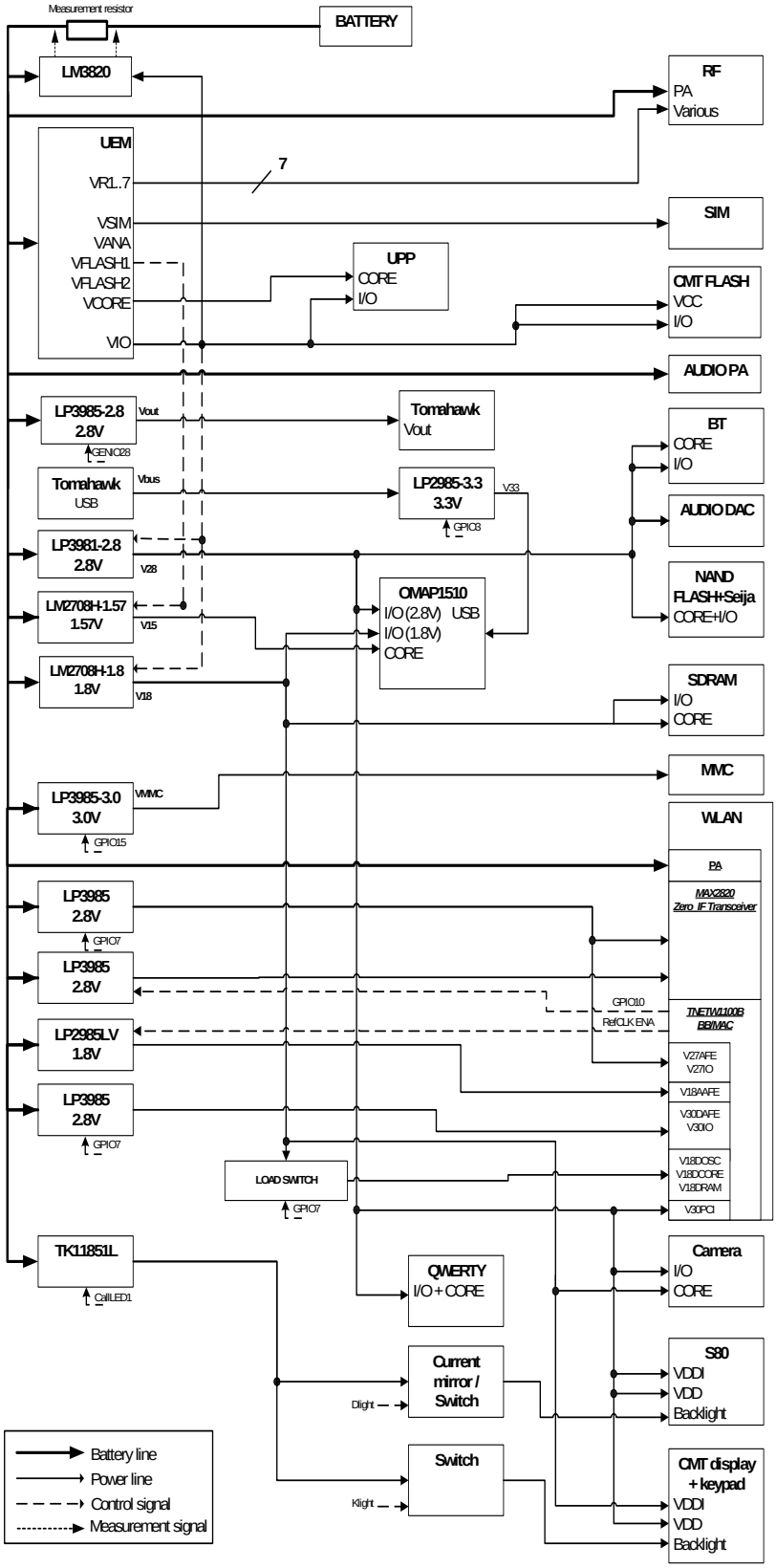
Note1: Values roughly estimated

WLAN MAC takes care of the transitions between Doze and Active mode. It also automatically controls the radio active modes (transmit and receive). These transitions are initiated by MAC protocol state machine. For example, mode change is initiated when the host starts data transfer or when the MAC decides to listen for incoming beacons.

Energy Management

Energy Management covers both CMT and APE sides. WLAN energy management is considered to be part of WLAN subsystem. Battery and charging functions are integrated into CMT Universal Energy Management (UEM) ASIC. UEM includes also all needed regulators for CMT BB and RF. APE side has its own discrete power supplies.

Figure 10:Power distribution diagram

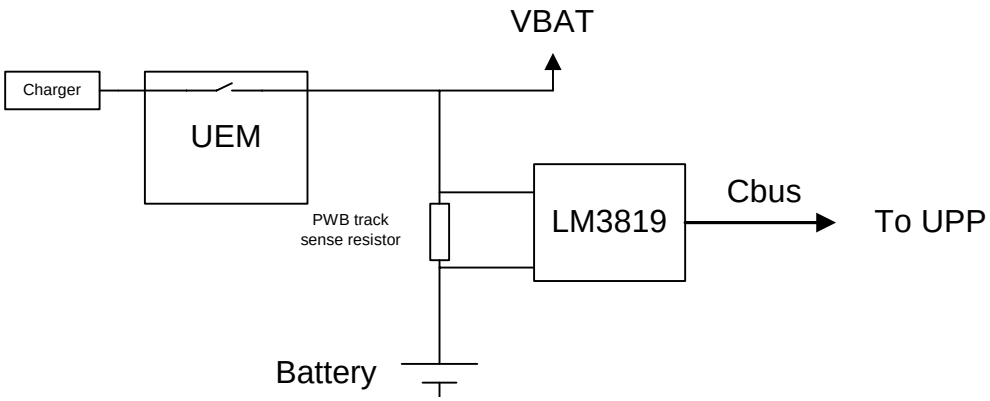


CMT EM

UEM includes following blocks:

- Baseband regulators (6 different LDOs)
- RF regulators (6 different 2.78V LDOs, 4.75V LDO and two current regulators)
- Power up/down logic (state machine).
- Charger switch and control

LM3819 (=Zocus-C) is the current measurement chip used for phone and charging current measurement. It can be used to estimate the battery charge level presented as battery bars on the display. Results are read with CBUS interface to the UPP.



APE EM

APE side EM HW consists of several discrete regulators (listed shortly below):

- Two DC/DC converters for generating 1.57V and 1.8V to OMAP1510 and SDRAM and WLAN core.
- One linear regulator for 2.8V APE side logic, NAND, etc.
- One 3.0V linear regulator for powering of MMC card.
- One 3.3V linear regulator for powering the USB block of OMAP1510.

Battery

1300 mAh Li-Po battery pack BP-5L is used in RA-2/3.

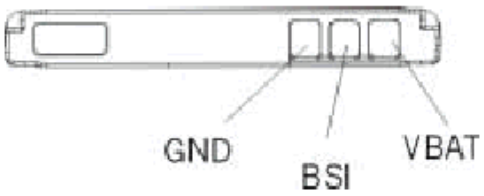
Table 5: BP-5L characteristics

Description	Value
Nominal discharge cut-off voltage	3.1V
Nominal battery voltage	3.6V
Nominal charging voltage	4.2V

Table 6: Pin numbering of battery pack

Signal name	Pin number	Function
VBAT	1	Positive battery terminal
BSI	2	Battery capacity measurement (fixed resistor inside the battery pack)
GND	3	Negative/common battery terminal

Figure 11:Battery pack contacts



Temperature and capacity information is needed for charge control.

The BSI fixed resistor value indicates type and default capacity of a battery.

NTC-resistor that measures the battery temperature is located inside the phone on the engine PWB. This resistor is connected to the UEM BTEMP –line.

BSI resistor is connected to the battery connector pin. Phone has 100 kOhm pull-up resistor for the line so that it can be read by A/D input in the phone.

Table 7: BSI Resistor Values

Parameter	Min	Typ	Max	Unit	Notes
Battery size indicator resistor BSI		100		kOhm	Battery size indicator for 1300 mAh battery (BP-5L), Tolerance +/- 1%
NTC thermistor BTEMP (inside phone)		47		kOhm	Battery temperature indicator (NTC pulldown) 47kOhm +/- 5% @ 25C
		4000		Ohm	Beta value (B). Tolerance ”5%, 25C / 85C

Charging

RA-2/3 supports all DCT4 chargers. 3-wire chargers are supported, but 3-wire charging is not. In practice, this means that the 3-wire chargers are internally connected (charger control wire connected to GND) as 2-wire chargers. 1Hz PWM signal is used to control UEM's charge switch.

Backup battery and RTC

Rechargeable backup battery is used for keeping real time clock running in case the main battery is either removed or the power level is below the cutoff limit.

Real Time Clock (RTC), crystal oscillator and backup battery circuitry are inside UEM. Two regulators are used to provide needed voltages for external backup supply and backup battery charging: VRTC for internal clock circuitry and VBU for backup battery charging. The backup battery has voltage range VBACK = $2.0V_{min}$ – $3.2V_{typ}$ – $3.3V_{max}$ (charged to 3.2V and discharged down to 2.0V).

Display and keypad illumination

One DC-DC converter generates the voltage for displays and keypad illumination. The converter is able to supply cover display and keypad OR PDA display, but both cannot be active at the same time. UEM controls the DC-DC converter and selection of cover/PDA display under APE control. The brightness of both cover and PDA display can be adjusted with UEM PWM output. For further details, see RA-2/3 flex section.

Power up and system states

System starts automatically after the battery is inserted. The power button is connected to UEM PWRONX pin on the CMT side. This power button is only used for selecting operating mode and switching the RF part of the device ON and OFF when needed. APE is started when UEM releases a PURX-signal, which controls OMAP1510 processor reset input.

Power off happens in the lowest SW cutoff limit when UEM watchdog is not updated anymore by SW and after that PURX goes to reset and system power supplies are switched OFF. However also in this power OFF mode (BACK_UP mode in UEM) part of UEM is powered ON but for user the device is dead. Only way to wake up from this mode is to plug in the charger or replace empty battery with the charged one.

Operating modes

- NO_SUPPLY mode means that the main battery is not present or its voltage is too low (below UEM master reset threshold limit) and back-up battery voltage is too low.
- In BACK_UP mode the main battery is disconnected or empty but back-up battery has sufficient charge in it
- IN POWER_OFF mode the main battery is present and its voltage is over UEM master threshold limit. All regulators are disabled. Device can enter in Power Off – mode e.g. due to thermal shutdown or watchdog elapsing or VBAT falling below VCOFF-.
- RESET mode is a synonym for start-up sequence and contains in fact several modes. In this mode certain regulators and system oscillators are enabled and after they have stabilized, the system reset (PURX) is released and PWR ON mode entered.
- In POWER_ON mode SW is running and controlling the system
- SLEEP mode is entered only from PWR ON mode when system activity is low. CMT and APE sides can be in sleep mode independently from each other.

Power up sequence

RESET mode can be entered in three ways: by inserting the battery or charger, or by RTC alarm.

System Connector

RA-2/3 supports usage of Pop-Port™ bottom connector. This means support for Pop-Port™ stereo and mono headsets with and without ACI, USB cable.

Pop-Port consists of a charging plug socket and system connector. The Pop-Port is a feature-based interface. The accessory contains information about its features (ACI ASIC) and it is detected with a fully digital detection procedure.

FBUS accessories are not supported.

Pop-Port™ connector includes VOUT pin, which is 2.78V/70mA output to accessories. VOUT voltages are: 2.43V(min.) and 2.86V(max.). In RA-2/3 2.8V linear regulator is used to supply accessories. Regulator output current capability is 150mA.

Four new functions are introduced with the system connector interface:

- Accessory control interface (ACI)
- Power out
- Stereo audio output
- Universal serial bus (USB)

Table 8: Pop-port™ functions

Function	Note
Charging	Pads for 2-wire charging in cradles
Audio	4-wire fully differential stereo audio output
Power supply for accessories	2.78V/70mA output to accessories
ACI (Accessory Control Interface)	Accessory detection/removal & controlling
FBUS	Standard FBUS, Fast FBUS *Note! RA-2/3 does not support accessories using FBUS serial interface.*
USB (default)	USB v.2.0 device mode (full speed 12M)

Figure 12:Pop-Port™ connections

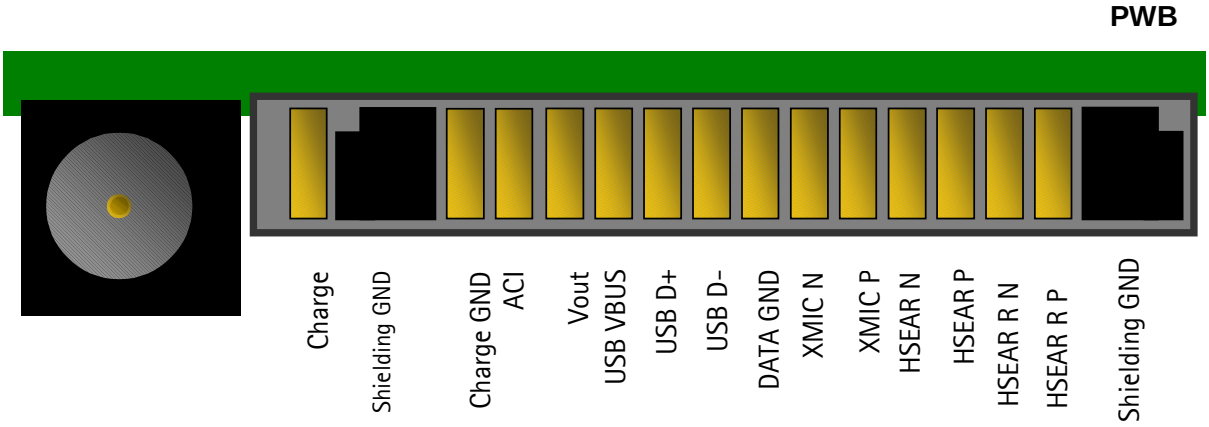


Table 9: Pop-port™ connections

Pin #	Signal	Note
1	VCHAR	
2	GND	Charge ground
3	ACI	Insertion & removal detection /Serial data bi-directional 1 kbit/s
4	Vout	200mW
5	USB VBUS	
6	USB D+/FBUS RX	
7	USB D-/FBUS TX	
8	USB data GND	Data ground
9	XMIC N	Negative audio in signal
10	XMIC P	Positive audio in signal
11	HSEAR N	Negative audio out signal. Max bandwidth from the phone
12	HSEAR P	Positive audio out signal. Max bandwidth from the phone
13	HSEAR R N	Not connected or grounded in mono.
14	HSEAR R P	Not connected or grounded in mono.

Universal Serial Bus (USB)

The USB interface of OMAP1510 supports the implementation of a full speed device, fully compliant to USB2.0 standard. RA-2/3 uses an integrated USB transceiver.

Accessory Control Interface (ACI)

ACI (Accessory Control Interface) is a point-to-point, bi-directional serial bus. ACI has two main features: 1) detecting the insertion and/or removal of an accessory device 2) acting as a data bus. A third function provided by ACI is to identify and authenticate a specific accessory which is connected to the system connector interface.

All accessories cause *headint* interrupt when connected to or disconnected from the system connector. The insertion of an accessory generates a Headint interrupt by pulling the ACI line down. When no accessory is present, the UEM's internal Headint pull-up resistor keeps the line high.

All accessories have common detection start sequence, when phone gets headint interrupt from high to low transition in ACI pin.

VOUT (Accessory Voltage Regulator)

An external LDO Regulator is needed for accessory power supply purposes. All ACI-accessories require this power supply. Regulator input is connected to the battery voltage VBAT and output is connected to the Vout pin. Regulator is controlled via UPP (On/Off-function).

HookInt

The hook signal is generated by creating a short circuit between the headset microphone signals. An LP-filter is needed on the HookInt input to filter the audio signal. In this mode, the earpiece signal on the HF and HFCM pins is in the opposite phase. The earpiece is driven differentially.

DC-plug

RA-2/3 uses a 3.5mm DC-plug. 3-wire chargers are supported, but 3-wire charging is not. In practice this means that the 3-wire chargers are internally connected (charger control wire connected to GND) as 2-wire chargers. 1Hz PWM signal is used to control UEM's charge switch.

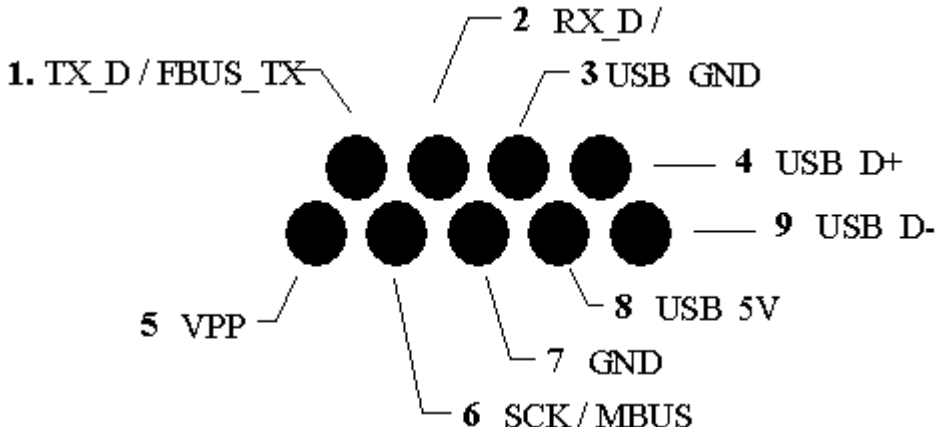
VCHAR pins of system connector

The VCHAR and ChargeGND pin are directly connected to the normal charger lines of the DC-plug.

After Sales Interface

Test pads are placed on engine PWB on battery side for service flashing and testing purposes.

Figure 13: Pin assignment in test pattern



User Interface

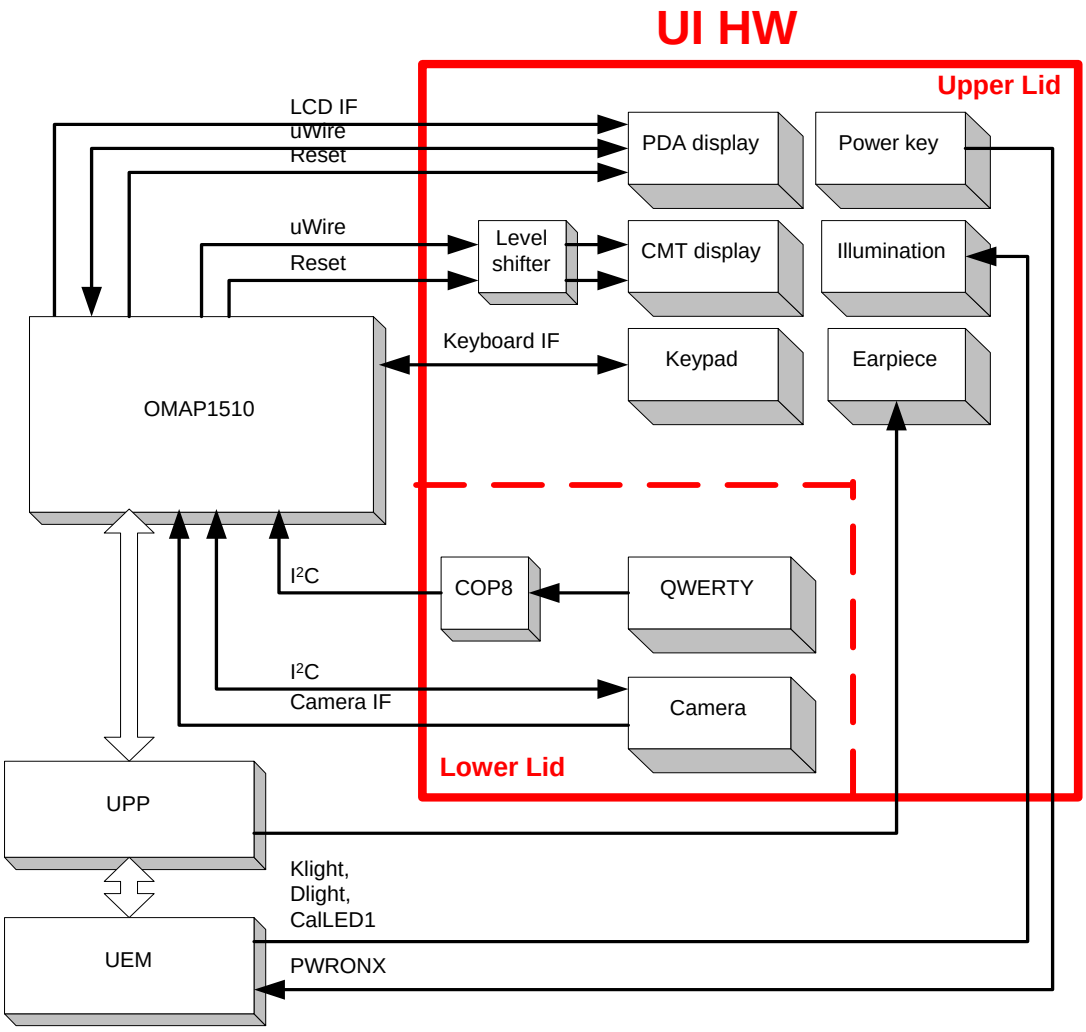
1BV is the UI flex module of RA-2 & RA-3 (US variant) communicators locating on the upper lid and connecting the following functional blocks to phone engine:

- PDA display
- CMT display
- CMT keypad
- Power key
- Illumination
- Earpiece

In addition to the actual components to provide the needed functionality, there are some components to filter out possible EMI/ESD disturbance. Figure 14, “Block Diagram of UI HW” shows a block diagram of the UI HW of RA-2/3.

The HW UI is based on APE chip (OMAP1510).

Figure 14:Block Diagram of UI HW



Component placement and FPWB outline of 1BV

1BV FPWB board size is 150x70mm. It has a double-layer structure. Hinge part is single layer. All the components are placed on one side of the 1BV FPWB. Figure 15, “Main components of 1BV” shows the main components and all the test points of the 1BV module.

Figure 15:Main components of 1BV

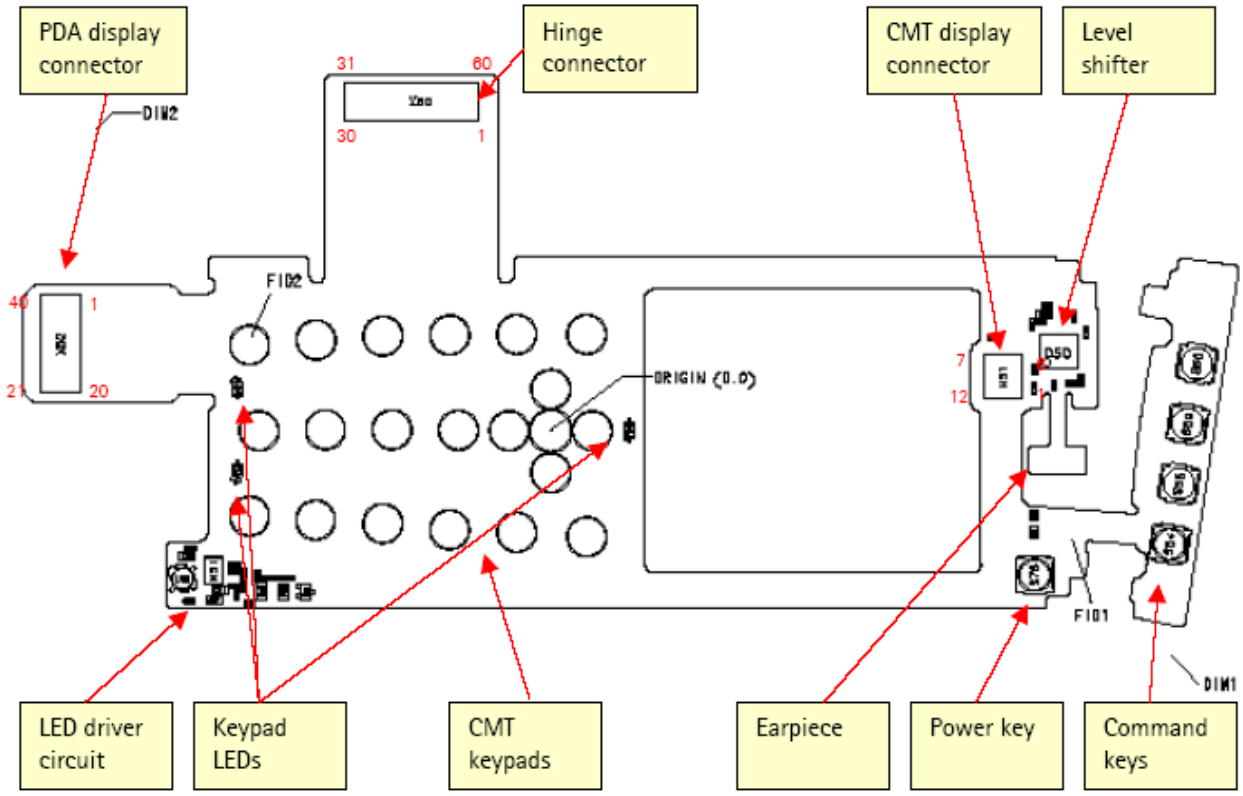
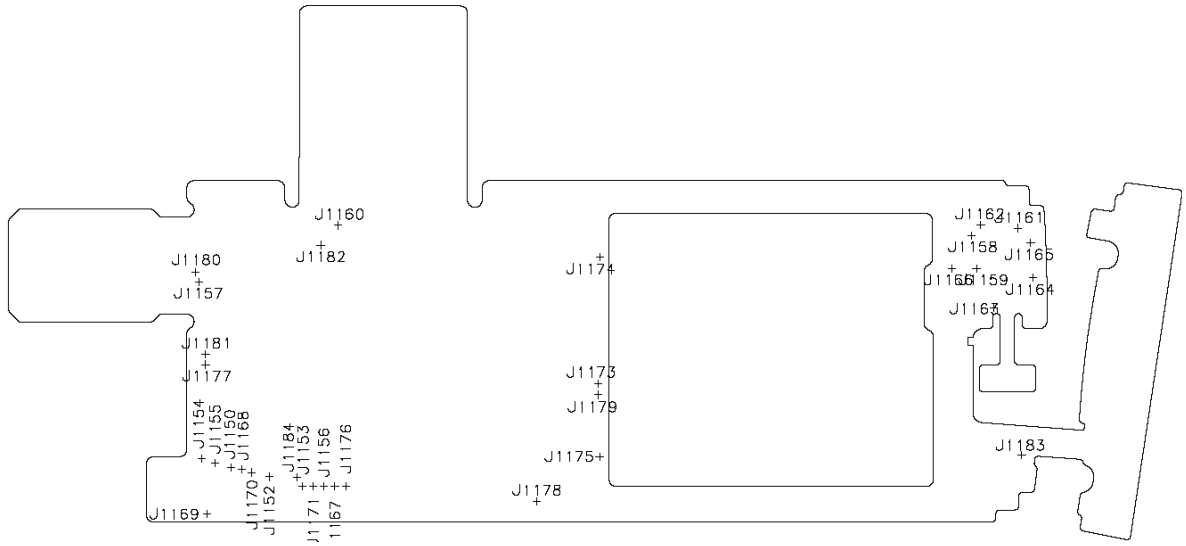


Figure 16:Test points of 1BV module



Hinge connector

Hinge connector (NMP code 546Y131) is a 60-pin board-to-board type connector with 0,5mm pitch, which connects flex module to the engine module. Table 10, “Interface signals of hinge connector” shows all the signals through hinge area of the flex.

Table 10: Interface signals of hinge connector

Pin #	Signal name (Engine)	Voltage level	I/O/Z	Description
1	WIRE_nSCS0	0 – 2.8V	I	Uwire chip select for CMT display (active low)
2	KBC5	0 - 2.8V	I	Keyboard interface column line
3	KBC4	0 - 2.8V	I	Keyboard interface column line
4	KBC3	0 - 2.8V	I	Keyboard interface column line
5	KBC2	0 - 2.8V	I	Keyboard interface column line
6	GND	0V	-	Ground
7	GND	0V	-	Ground
8	GND	0V	-	Ground
9	GND	0V	-	Ground
10	KBC1	0 - 2.8V	I	Keyboard interface column line
11	LCD_PCLK	0 - 2.8V	I	Display interface pixel clock for PDA display
12	LCD_PXL11	0 - 2.8V	I	Display interface data for PDA display
13	LCD_PXL12	0 - 2.8V	I	Display interface data for PDA display
14	LCD_PXL13	0 - 2.8V	I	Display interface data for PDA display
15	LCD_PXL14	0 - 2.8V	I	Display interface data for PDA display
16	GND	0V	-	Ground
17	GND	0V	-	Ground
18	LCD_PXL15	0 - 2.8V	I	Display interface data for PDA display
19	LCD_PXL5	0 - 2.8V	I	Display interface data for PDA display
20	LCD_PXL6	0 - 2.8V	I	Display interface data for PDA display
21	LCD_AC	0 - 2.8V	I	Display interface data enable for PDA display
22	LCD_HSYNC	0 - 2.8V	I	Display interface horizontal synchronization for PDA display

23	GND	0V	-	Ground
24	GND	0V	-	Ground
25	GND	0V	-	Ground
26	LCD_VSYNC	0 - 2.8V	I	Display interface horizontal synchronization for PDA display
27	WIRE_SDI	0 – 2.8V	O	Uwire serial data output from PDA display
28	WIRE_SDO	0 – 2.8V	I	Uwire serial data input for both displays
29	WIRE_nSCS3	0 – 2.8V	I	Uwire chip select for PDA display (active low)
30	GPIO13	0 - 2.8V	I	Reset for PDA display
31	GND	0V	-	Ground
32	LCD_PXL4	0 - 2.8V	I	Display interface data for PDA display
33	LCD_PXL3	0 - 2.8V	I	Display interface data for PDA display
34	LCD_PXL2	0 - 2.8V	I	Display interface data for PDA display
35	LCD_PXL1	0 - 2.8V	I	Display interface data for PDA display
36	LCD_PXL0	0 - 2.8V	I	Display interface data for PDA display
37	LCD_PXL10	0 - 2.8V	I	Display interface data for PDA display
38	LCD_PXL9	0 - 2.8V	I	Display interface data for PDA display
39	LCD_PXL8	0 - 2.8V	I	Display interface data for PDA display
40	LCD_PXL7	0 - 2.8V	I	Display interface data for PDA display
41	V28	2.716 – 2.884V	-	Supply voltage for CMT display
42	KBR4	0 - 2.8V	O	Keyboard interface row line
43	WIRE_SCLK	0 – 2.8V	I	Uwire serial clock for both displays
44	GNDKBC0	0V0 - 2.8V	-I	GroundKeyboard interface column line
45	KLIGHT	0 - 3.6V	I	Enable for CMT illumination
46	DLIGHT	0 - 3.6V	I	Enable for PDA display illumination
47	CALLED1	0 - 2.8V	I	On/off for LED driver
48	VBAT	3.0 – 4.2V	-	Battery voltage for illumination
49	KBR3	0 - 2.8V	O	Keyboard interface row line
50	KBR2	0 - 2.8V	O	Keyboard interface row line
51	PWRONX	0 - 2.8V	O	Power key output

52	KBR0	0 - 2.8V	O	Keyboard interface row line
53	GPIO12	0 - 2.8V	I	Reset for CMT display
54	EARP	1.4V DC, 35-222mV(rms) AC	I	Audio for earpiece
55	EARN	1.4V DC, 35-222mV(rms) AC	I	Audio for earpiece
56	KBR1	0 - 2.8V	O	Keyboard interface row line
57	V18	1.71 – 1.89V	-	Supply voltage for CMT display and level shifters
58	V28	2.716 – 2.884V	-	Supply voltage for CMT display
59	GND	0V	-	Ground
60	GND	0V	-	Ground

PDA display

PDA display is an S80L display module, 640(H) x RGB(H) x 200(V) transflective active matrix colour LCD. It is capable of showing 65536 colours (5xR, 6xG, 5xB). It incorporates a backlight system with 2x3 white LEDs connected in series.

The display has the following on-chip features: contrast control, DC/DC converter, temperature compensation and N-line inversion for low cross talk CMOS compatible inputs/outputs.

The complete display module includes LCD glass, flex cable (FPWB), driver IC and illumination system.

Interface

The PDA display has two interfaces: 16 data lines parallel video RGB interface ViSSI and optional 3-wire 9-bit serial interface LoSSI. Video interface is used for image data transfer (video and still) and serial interface is used for sending commands. GPIO13 is reset signal for PDA display.

The display is connected to the LCD interface of the OMAP1510 chip.

The interconnection between the LCD module and engine is implemented with a 40-pin board-to-board connector (NMP code 546B033).

All the signals go through the hinge flex and are filtered by EMI filters.

Table 11: Interface signals of PDA display.

Pin #	Signal name (LCD)	Signal name (Engine)	Voltage level	I/O/Z	Description
1	GND	GND	0V	-	Ground
2	VLED+	Vovp (LED Driver)	Variable ~12V	-	Voltage for LEDs

3	VLED1-	Vfb1 (LED Driver)	12 / 1V	-	Return line for LEDs 1
4	VLED2-	Vfb2 (LED Driver)	12 / 1V	-	Return line for LEDs 2
5	GND	GND	0V	-	Ground
6	VDDI	V28	2.8V	I, PSU	Logic power supply voltage
7	GND	GND	0V	-	Ground
8	GND	GND	0V	-	Ground
9	VDD	V28	2.8V	I, PSU	Analog power supply voltage
10	!RES	GPIO13	0 – 2.8V	I	Reset signal
11	!CS	WIRE_nSCS3	0 – 2.8V	I	Chip select signal
12	GND	GND	0V	-	Ground
13	SCLK	WIRE_SCLK	0 – 2.8V	I	Serial clock
14	DIN	WIRE_SDO	0 – 2.8V	I	Serial data input
15	DOUT	WIRE_SDIN	0 – 2.8V	O	Serial data output
16	GND	GND	0V	-	Ground
17	Vsync	LCD_VSYNC	0 – 2.8V	I	Vertical synchronization signal
18	Hsync	LCD_HSYNC	0 – 2.8V	I	Horizontal synchronization signal
19	DE	LCD_AC	0 – 2.8V	I	Data enable
20	GND	GND	0V	-	Ground
21	PCLK	LCD_PCLK	0 – 2.8V	I	Pixel clock signal
22	GND	GND	0V	-	Ground
23	R0	LCD_PXL11	0 – 2.8V	I	Image data input red, LSB
24	R1	LCD_PXL 12	0 – 2.8V	I	Image data input red
25	R2	LCD_PXL 13	0 – 2.8V	I	Image data input red
26	R3	LCD_PXL 14	0 – 2.8V	I	Image data input red
27	R4	LCD_PXL 15	0 – 2.8V	I	Image data input red, MSB
28	GND	GND	0V	-	Ground
29	G0	LCD_PXL 5	0 – 2.8V	I	Image data input green, LSB
30	G1	LCD_PXL 6	0 – 2.8V	I	Image data input green

31	G2	LCD_PXL 7	0 – 2.8V	I	Image data input green
32	G3	LCD_PXL 8	0 – 2.8V	I	Image data input green
33	G4	LCD_PXL 9	0 – 2.8V	I	Image data input green
34	G5	LCD_PXL 10	0 – 2.8V	I	Image data input green, MSB
35	GND	GND	0V	-	Ground
36	B0	LCD_PXL 0	0 – 2.8V	I	Image data input blue, LSB
37	B1	LCD_PXL 1	0 – 2.8V	I	Image data input blue
38	B2	LCD_PXL 2	0 – 2.8V	I	Image data input blue
39	B3	LCD_PXL 3	0 – 2.8V	I	Image data input blue
40	B4	LCD_PXL 4	0 – 2.8V	I	Image data input blue, MSB

CMT display

This section outlines the 128 x 128 transflective active matrix LCD with 65536 colours.

The display module includes:

- FPWB foil including connector and required passive components
- Display panel (glass) with COG drivers including display controller and 132 x132 x16 bit RAM
- Illumination system: light guide, optical sheets and LEDs

Interface

The display module is equipped with a DCT4 compatible LCD controller (Driver) with bi-directional 9-bit serial interface. The CMT LCD is connected to the uWire interface of the OMAP1510 chip. The maximum clock frequency of the OMAP1510 uWire is 3.0 MHz. GPIO12 is the reset signal for the CMT display.

Because of different logic levels of OMAP (2,8 V) and display (1,8 V), level shifters are used in the following signal lines: SDA, CSX, RESX and SCL.

The interconnection between the LCD module and engine is implemented with a 12-pin board-to-board connector (NMP code 546B047).

All the signals go through the hinge flex and are filtered by EMI filters.

Table 12: interface signals of CMT display.

Pin #	Signal name (LCD)	Signal name (Engine)	Voltage level	I/O/Z	Description
1	VLED-	Vfb (LED Driver)	12 / 0.4V	-	LED power supply (cathode)

2	VDDI	V18	1.8V	I, PSU	Supply voltage for digital circuits
3	GND	GND	0V	-	Ground
4	SDA	WIRE_SDO	0 – 1.8V (LCD)	I/O	Bi-directional serial interface data but only used as unidirectional.1)
			0 – 2.8V (OMAP1510)		
5	CSX	WIRE_nSCS0	0 – 1.8V (LCD)	I	Chip select (active low) 1)
			0 – 2.8V (OMAP1510)		
6	GND	GND	0V	-	Ground
7	TE	-	0 – 1.8V	O	Tearing Effect signal
8	RESX	GPIO12	0 – 1.8V (LCD)	I	Reset signal (active low) 1)
			0 – 2.8V (OMAP1510)		
9	SCL	WIRE_SCLK	0 – 1.8V (LCD)	I	Serial interface clock 1)
			0 – 2.8V (OMAP1510)		
10	GND	GND	0V	-	Ground
11	VDD	V28	2.8V	I, PSU	Power supply for analogue circuits
12	VLED+	Vovp (LED Driver)	Variable ~12V	-	LED power supply (anode)

Note! Level shifter used.

CMT keypad

The amount of keys in RA-2/3 on the lid side is 276. The keys are connected to the OMAP1510 keyboard interface, except the power key (NMP code 520B009), which is connected to PWRONX pin of UEM. Keyboard interface in OMAP1510 has a 6x5 matrix. The total amount of the keypad signals through hinge flex is 1211. Keyboard matrix can be seen in Table 13, “Keypad placement matrix.” Keys are divided into CMT keys and CBA Soft Command keys that are also called PDA keys (NMP code 520B009). CMT keys are on the topside of the lid and PDA keys are on the bottom side, next to the PDA display. All the signals go through EMI filters.

Table 13: Keypad placement matrix.

	Col 0	Col 1	Col 2	Col 3	Col 4	Col 5
Row 0	Special key	UP	CMT 1	CMT 2	CBA 1	CBA 2
Row 1		PUSH	SEND	END	CBA 3	CBA 4
Row 2		DOWN	1	2	3	*
Row 3		LEFT	4	5	6	0
Row 4		RIGHT	7	8	9	#

Table 14: OMAP1510 keypad interface

From	Signal Pin(s)	To	Signal Pin(s)	Levels	Description
OMAP1510	APE_KEYB(10:0)	Keyboard Matrix	Column(5:0)	0-2.8V	Keyboard control: Column
Keyboard Matrix	Row (4:0)	OMAP1510	APE_KEYB(10:0)	0-2.8V	Keyboard control: Row with external pull-up

Description of operation

A keyboard Interface in OMAP1510 consists of specific I/O pins, dedicated for the 6 columns X 5 rows keyboard connection.

The keyboard interface is composed of six column lines (output), KBC (5:0); and five row lines (input), KBR (4:0) with the capability to detect multiple key pressing.

When no key is pressed, KBD_INT remains high because of external pull up, once key(s) is (are) pressed, the corresponding row(s) and column(s) are shorted together, since KBC is set to low initially, therefore, KBD_INT is changed to low state and interrupt is generated that CPU will perform a scanning process to tell which key(s) are pressed.

In case of a determined key press SW must ensure is the key pressed or not by multi-read operation.

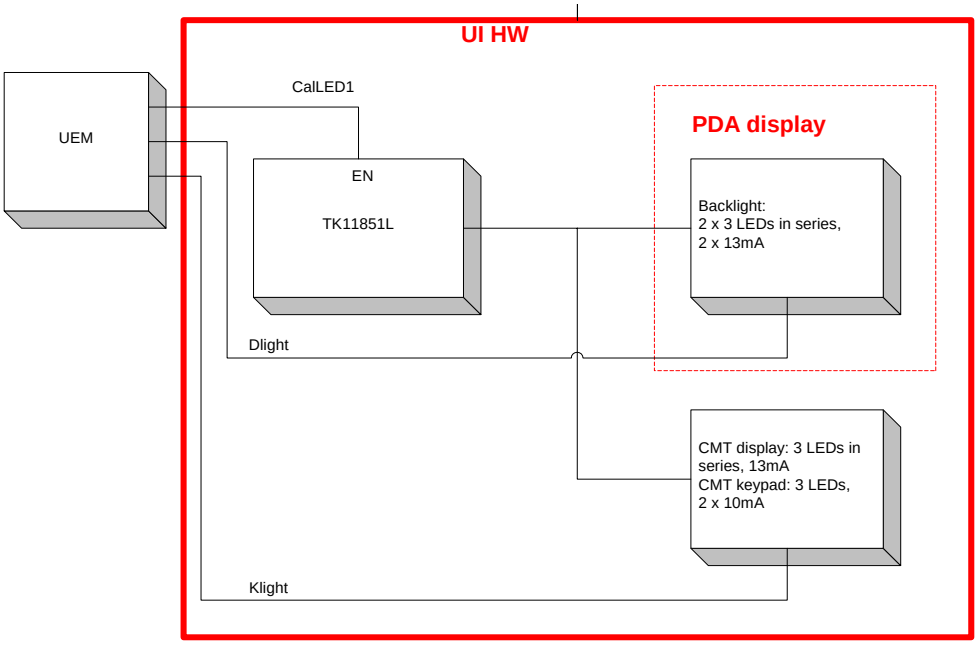
Illumination and drivers

The illumination includes:

- PDA display
- CMT display
- CMT keypad illumination

Block diagram

Figure 17: Block diagram of illumination.



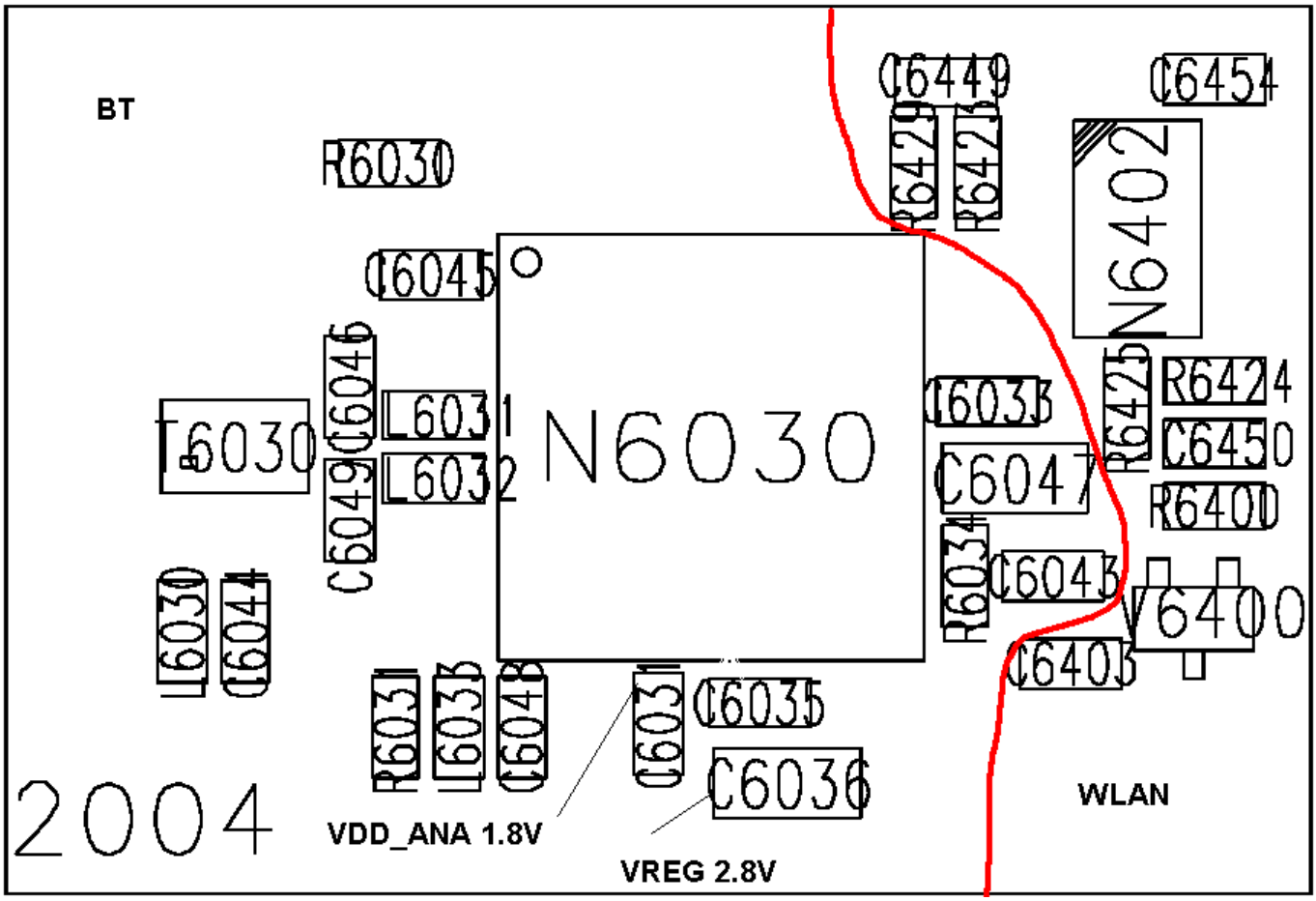
- S80L backlight
- Keypad backlight
- TK11851L: white LED driver for backlight
- UEM PWM signals Dlight and Klight are to turn on/off white LED circuits

Description of operation

There are 6 white LEDs for illumination built in S80L module. There are two LED chains connected in parallel. Each of these chains consists of three LEDs in series. Since the forward voltage drop, Vf, of each white LED is typically about 3.6 to 4V; a white LED driver is required to drive the LEDs for the desired performance. A current mirror (TBD) is used to ensure matched current for both LED chains. In the CMT display there are three LEDs connected in series. Common TK11851L driver is used for S80L display and for CMT display + keypad.

Bluetooth

Figure 18:RA-2/3 bluetooth component assembly (BT is on the bottom layout layer, but Z6400, N6403, N6404, C6400, C6403, C6422 are on the top layout layer(WLAN partition)

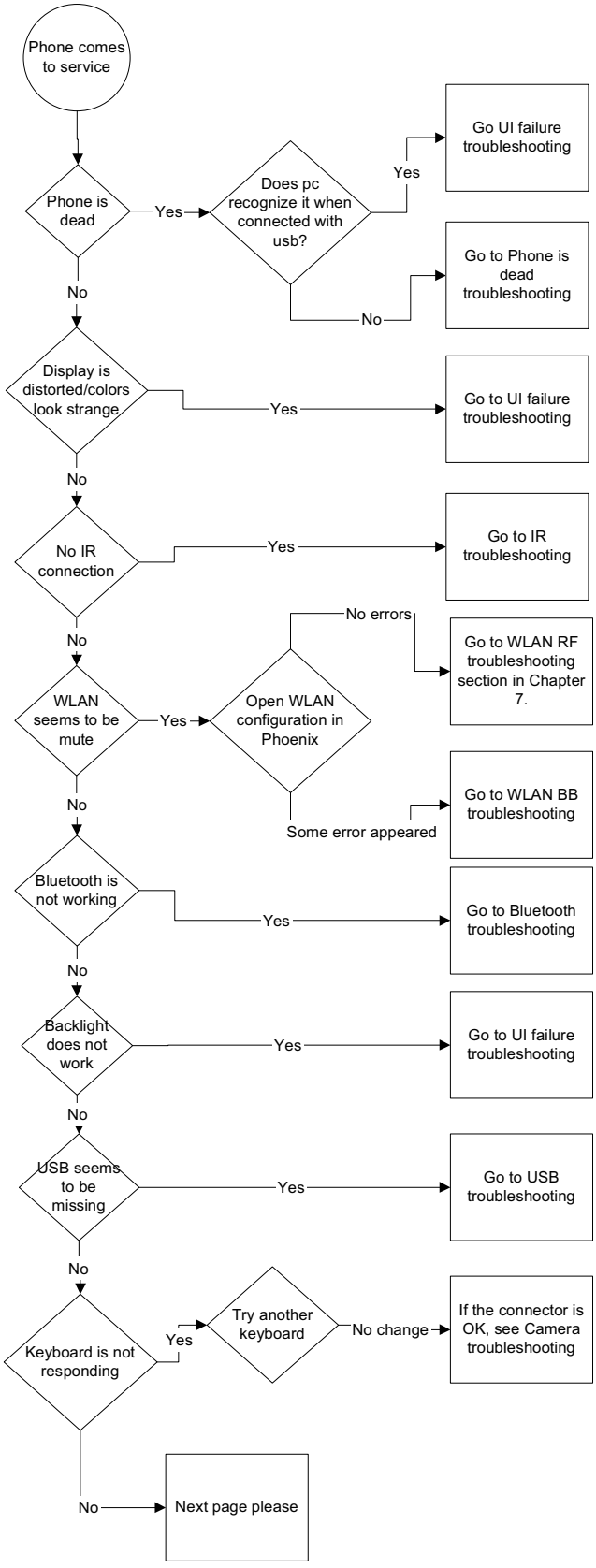


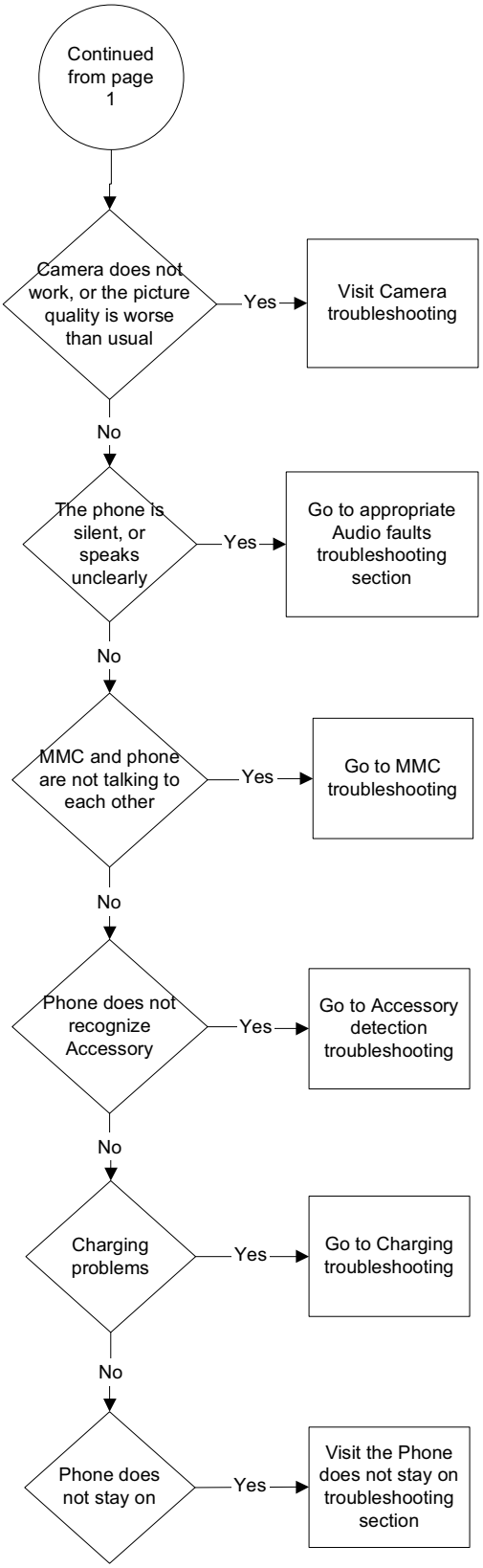
Baseband Troubleshooting

This section is intended to be a guide for localizing and repairing electrical faults in RA-2/3 baseband.

Before any service operation you must be familiar with the RA-2/3 product and module level architecture. You have to be also familiar with the RA-2/3 specific service tools such as the Phoenix service software, flashing tools and software.

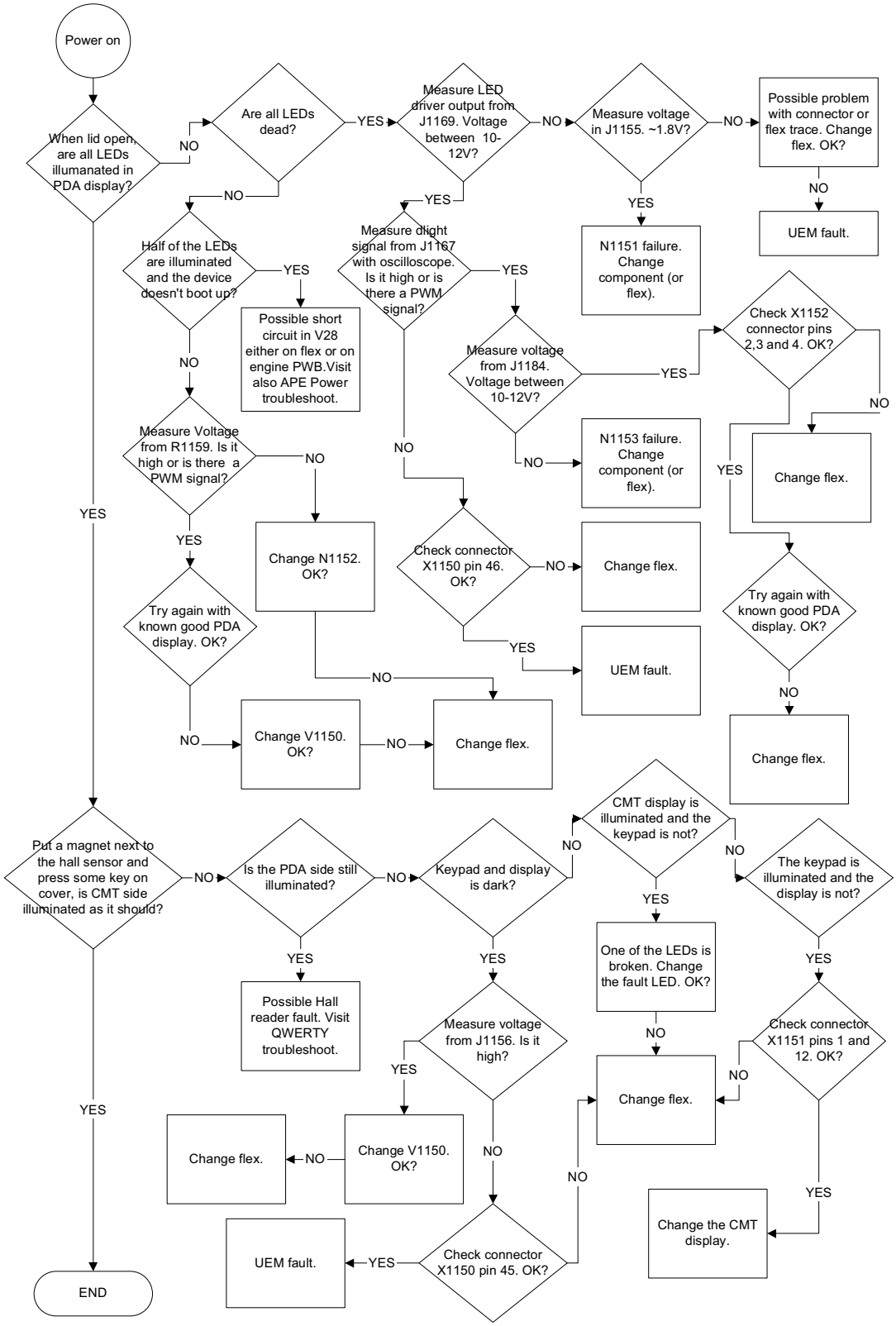
Top level flowchart



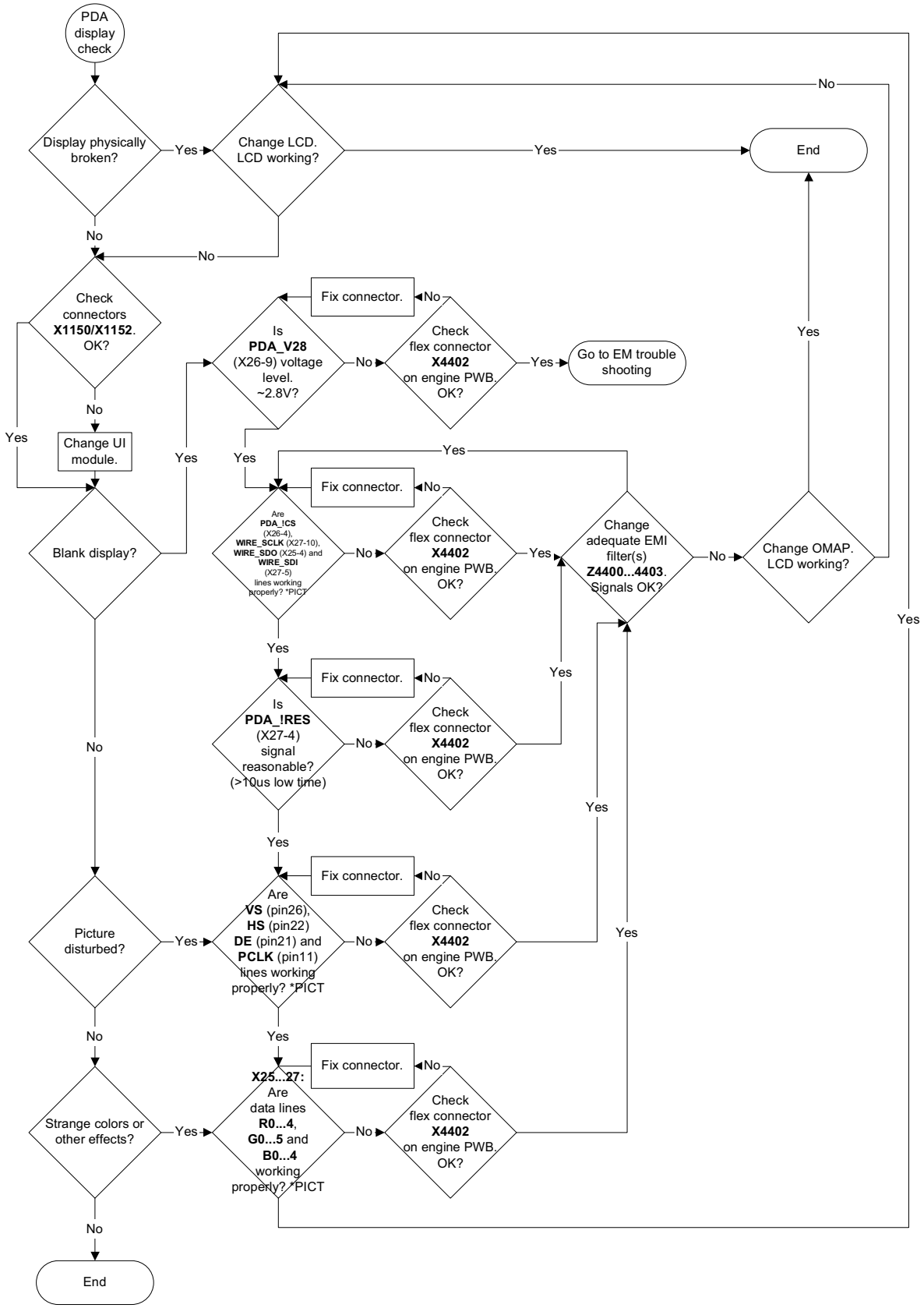


UI failure troubleshooting

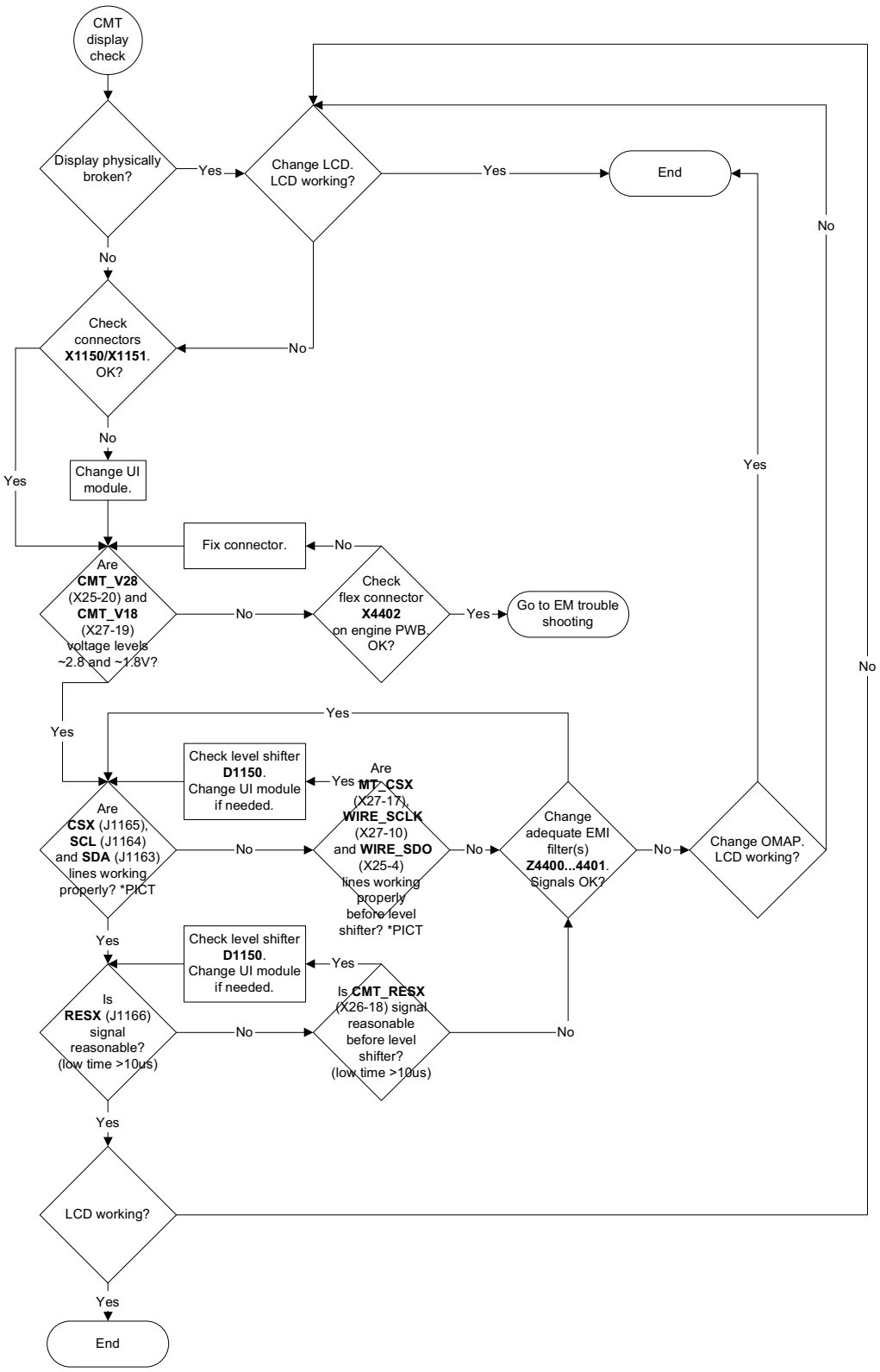
Display backlight dim or no backlight



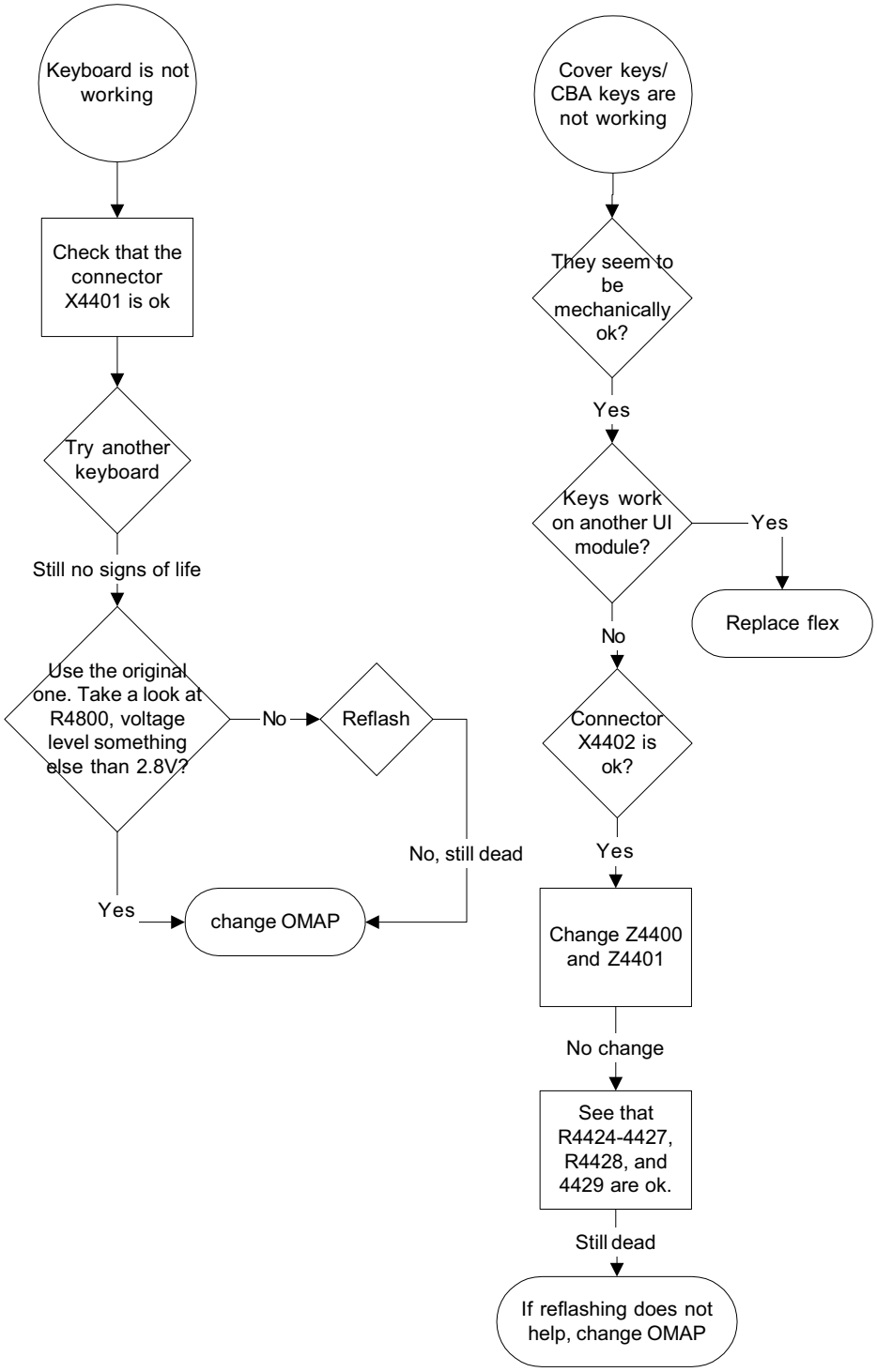
PDA display troubleshooting



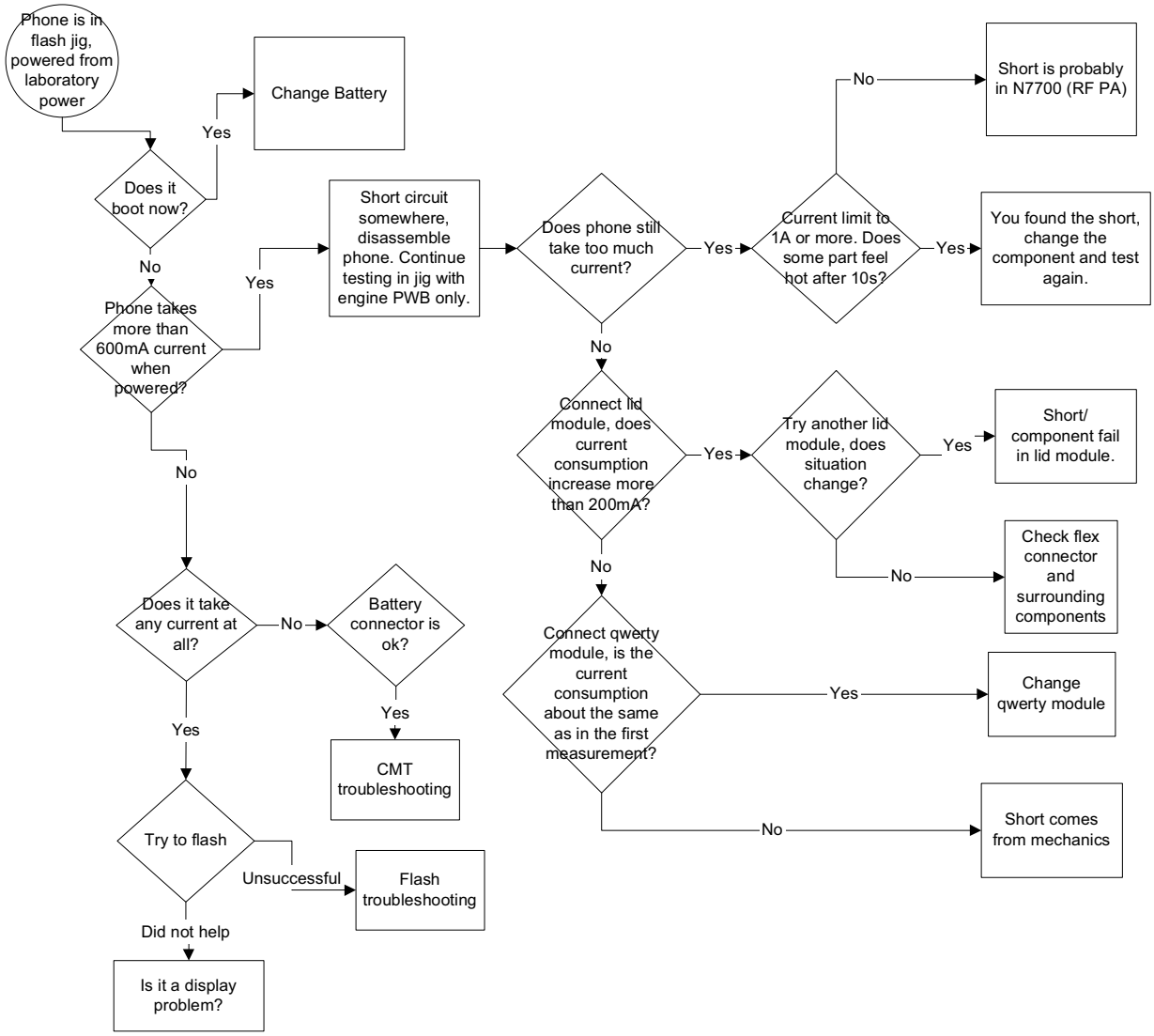
CMT display troubleshooting



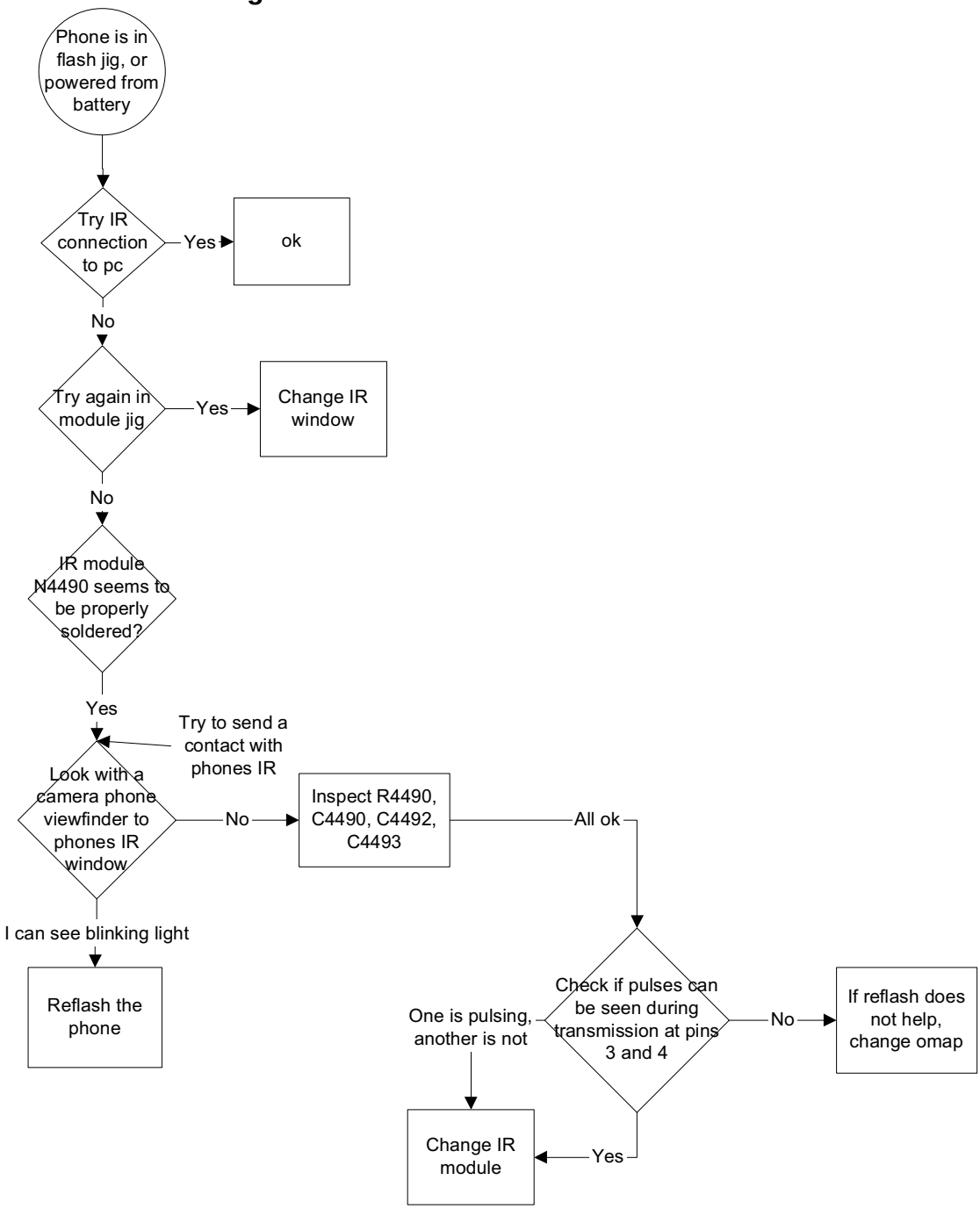
Keyboard malfunction



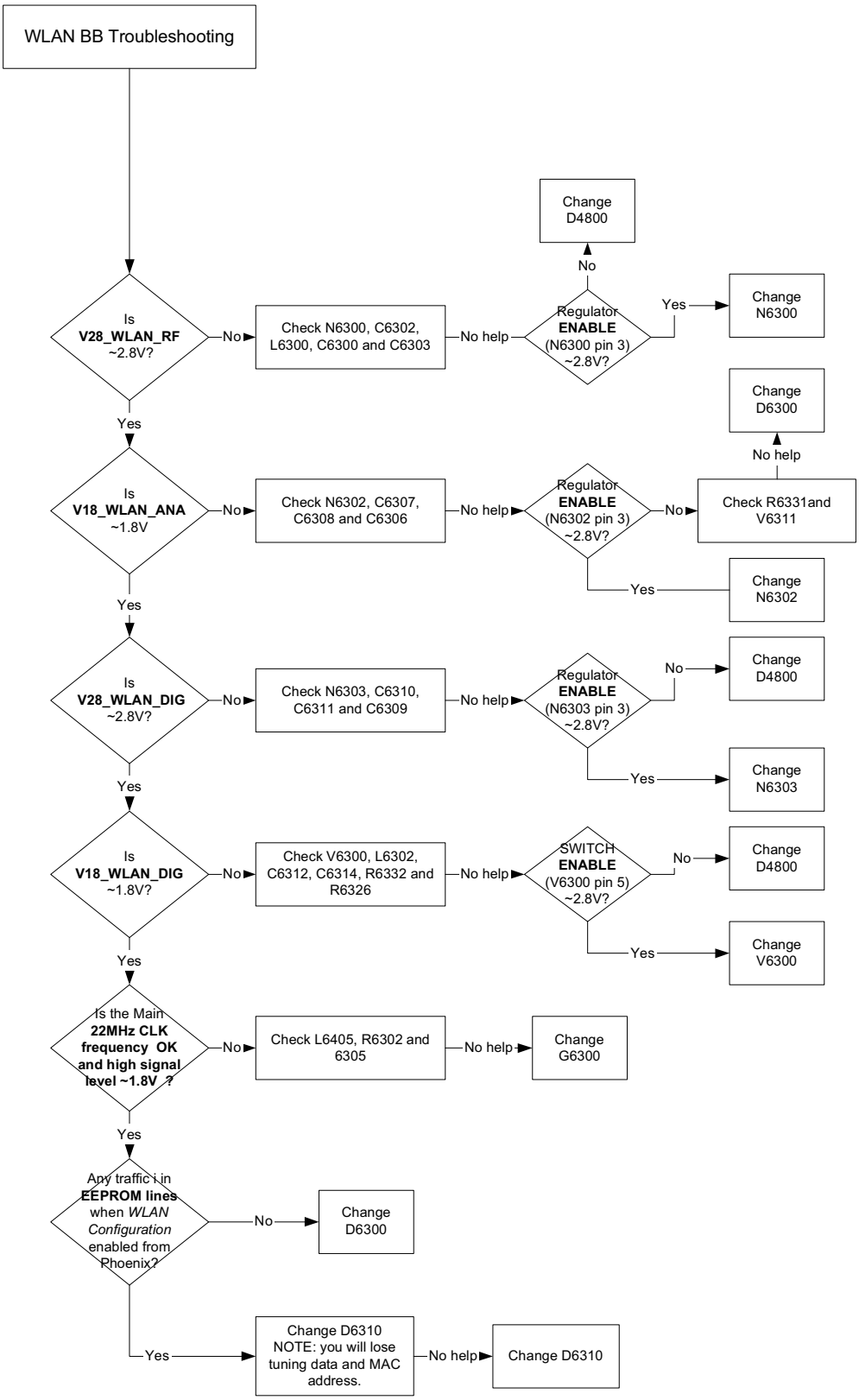
Phone is dead troubleshooting



IR troubleshooting



WLAN BB troubleshooting



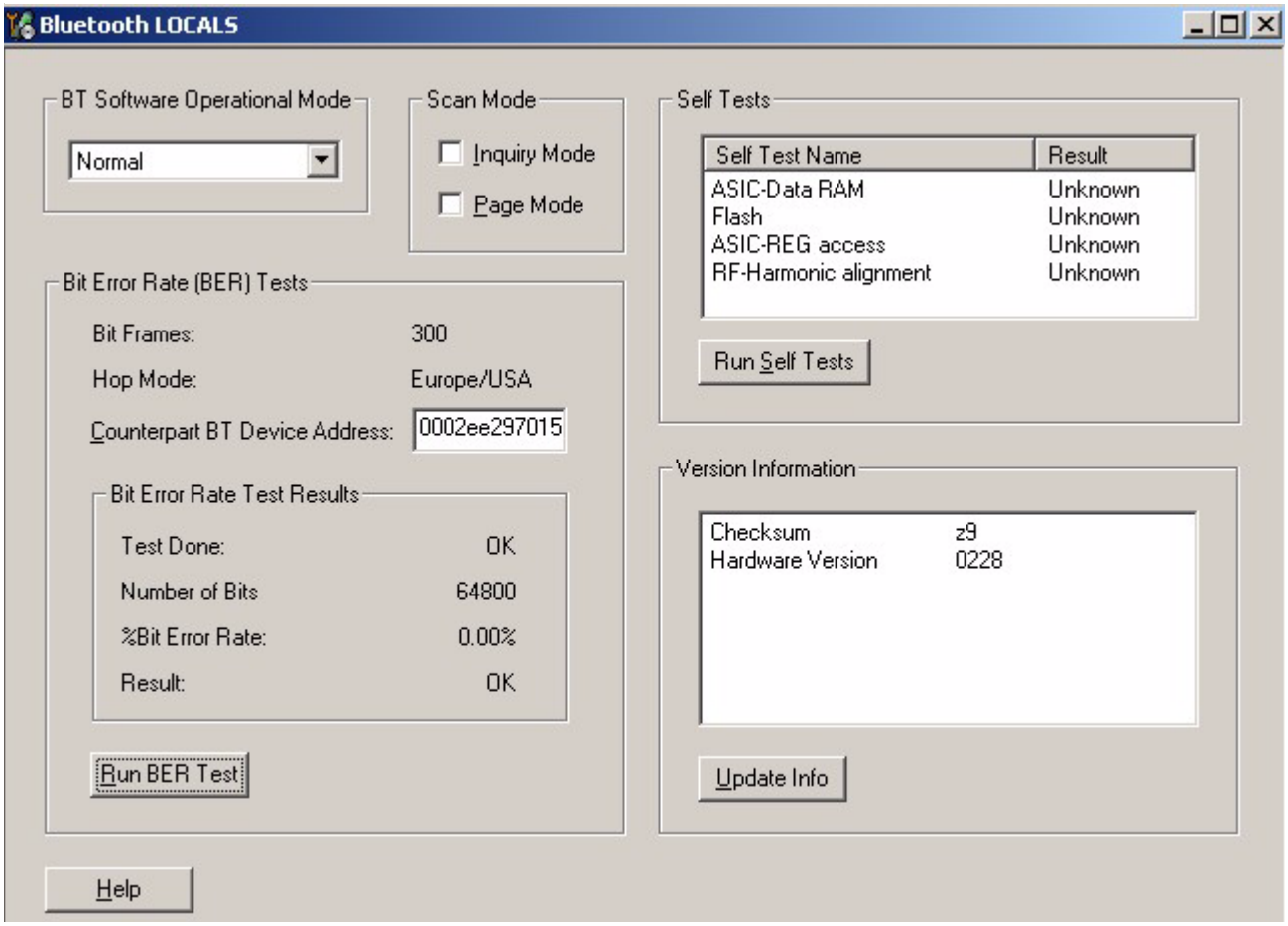
Bluetooth troubleshooting

Bluetooth settings for Phoenix

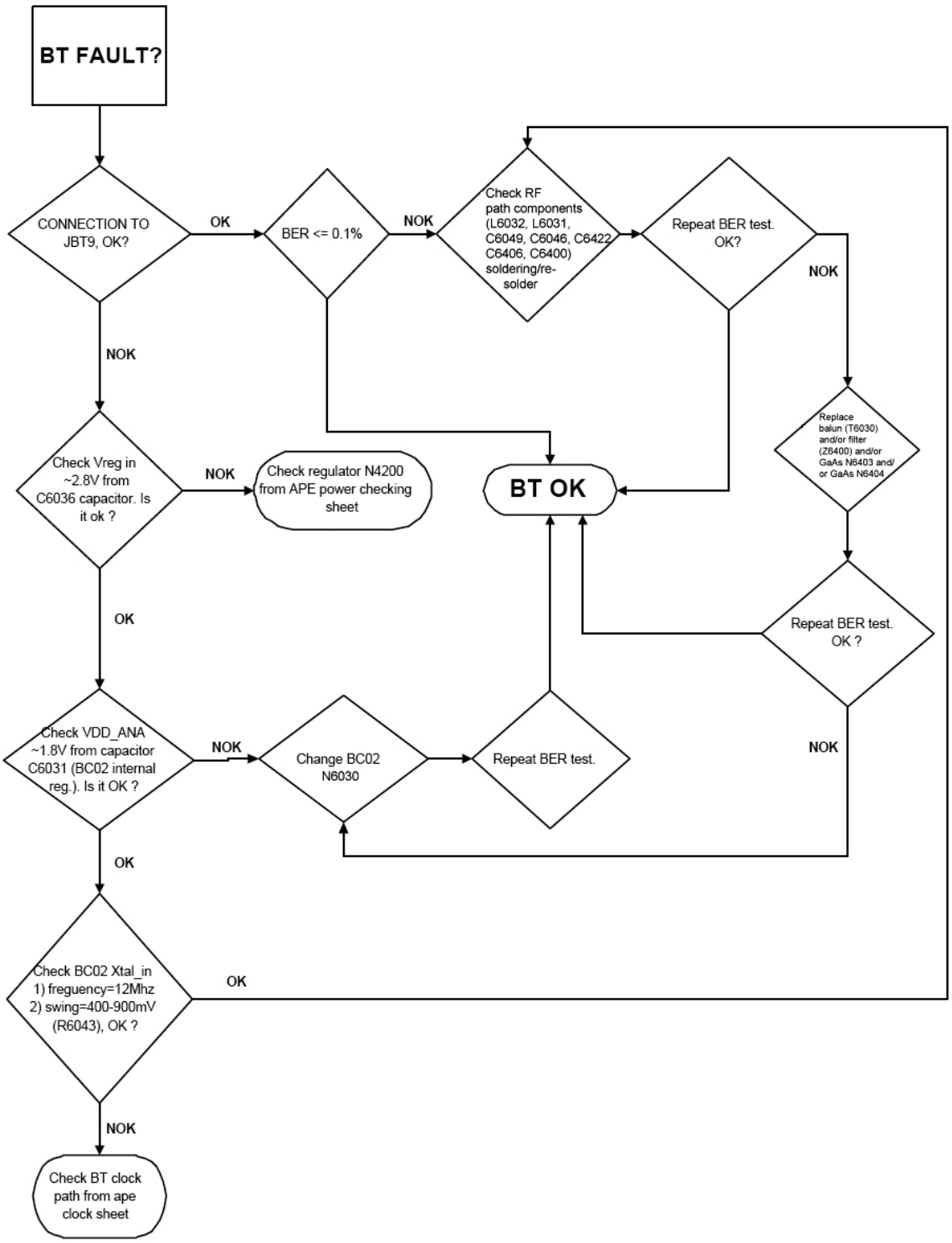
General setup:

1. Connect the phone to Phoenix in ‘local’ mode (From the File menu, choose Scan Product).
2. Choose: Testing --> Bluetooth LOCALS.
3. In the Bluetooth LOCALS window, set the JBT-9 box counterpart BT device address.
4. Place the JBT-9 box close to the BT antenna (within 10 cm) and click Run BER Test.

Figure 19:Example of Phoenix settings in Bluetooth troubleshooting



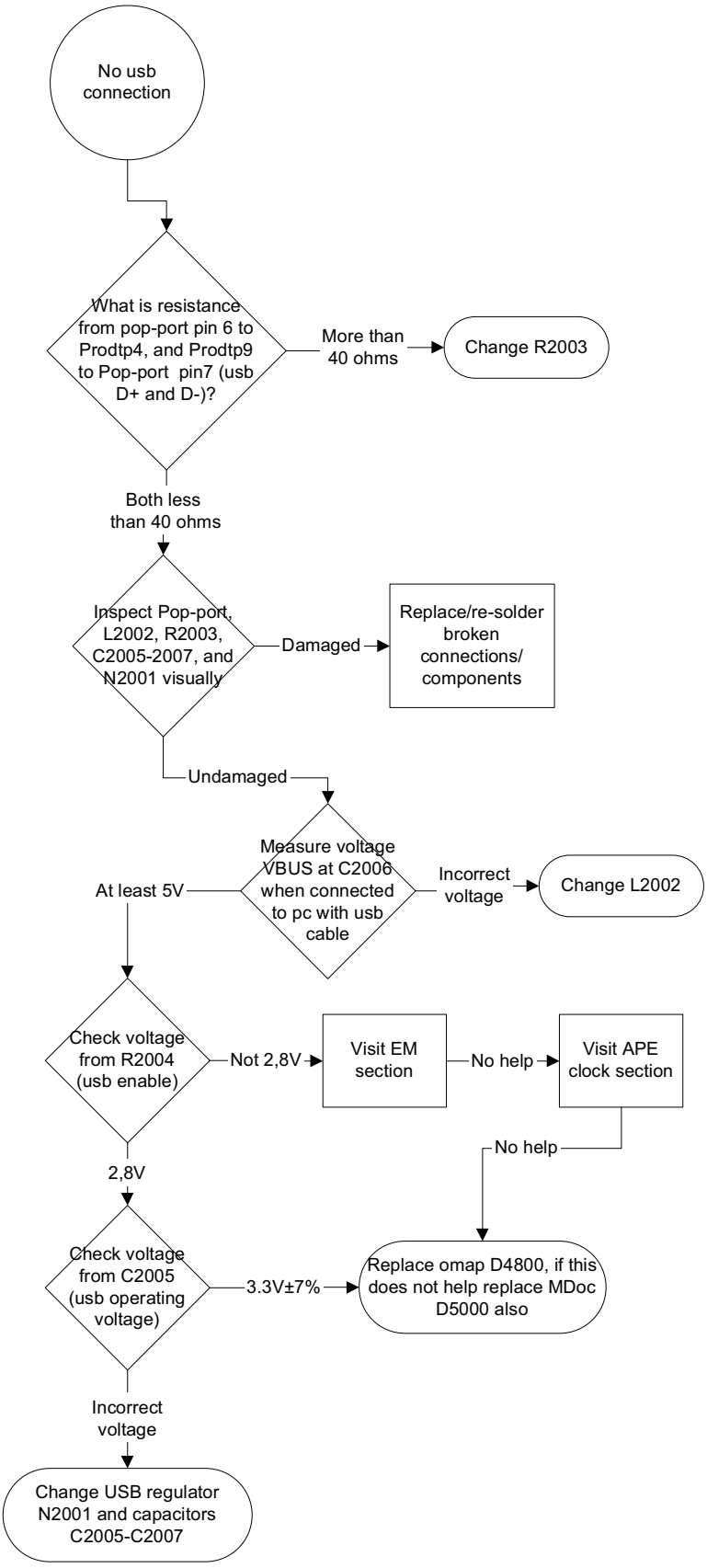
Bluetooth troubleshooting



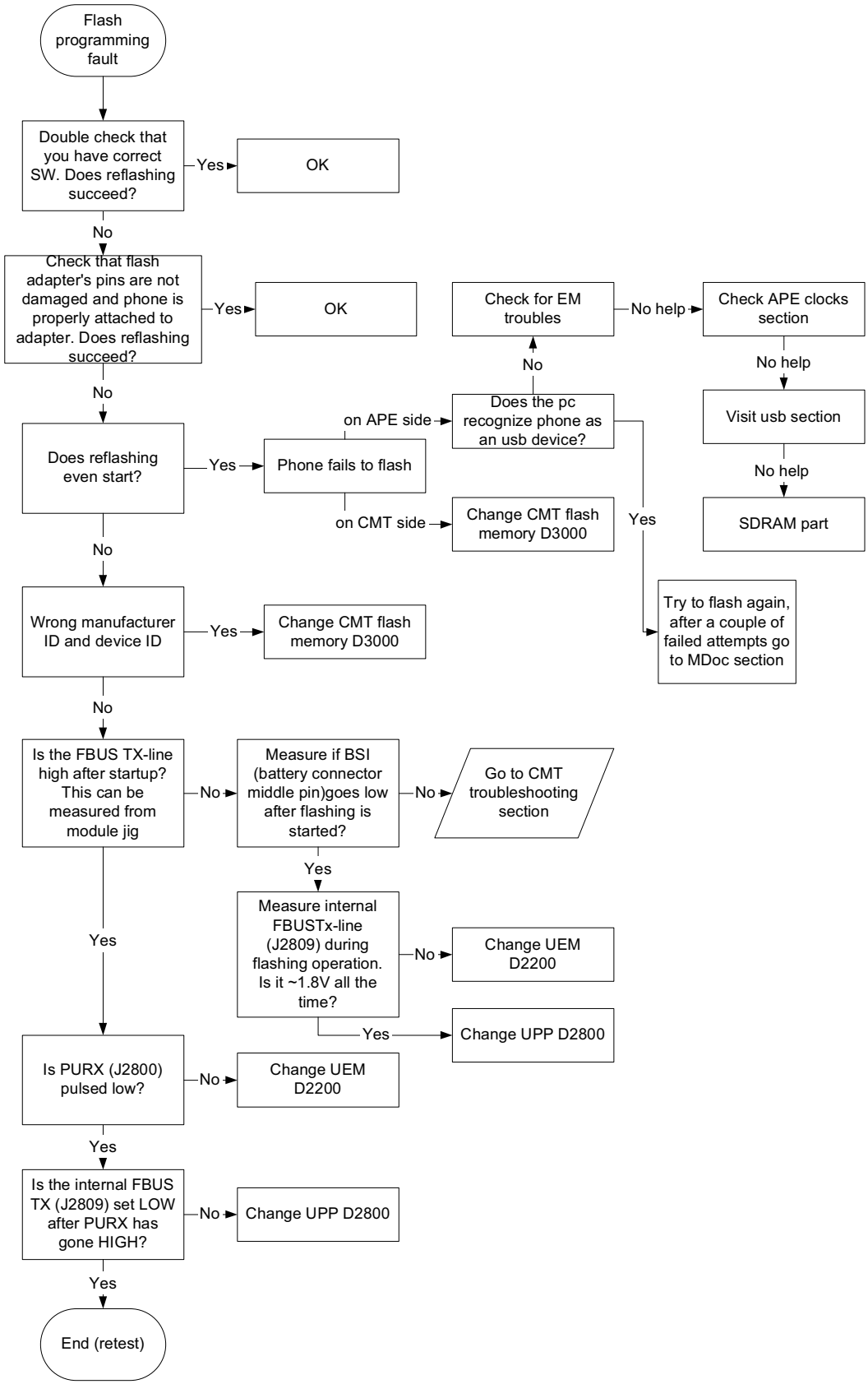
**If N6403 N6404, C6400, C6406, Z6400 are changed, WLAN tuning is also required.*

Check and measure other passive components visually, if needed.

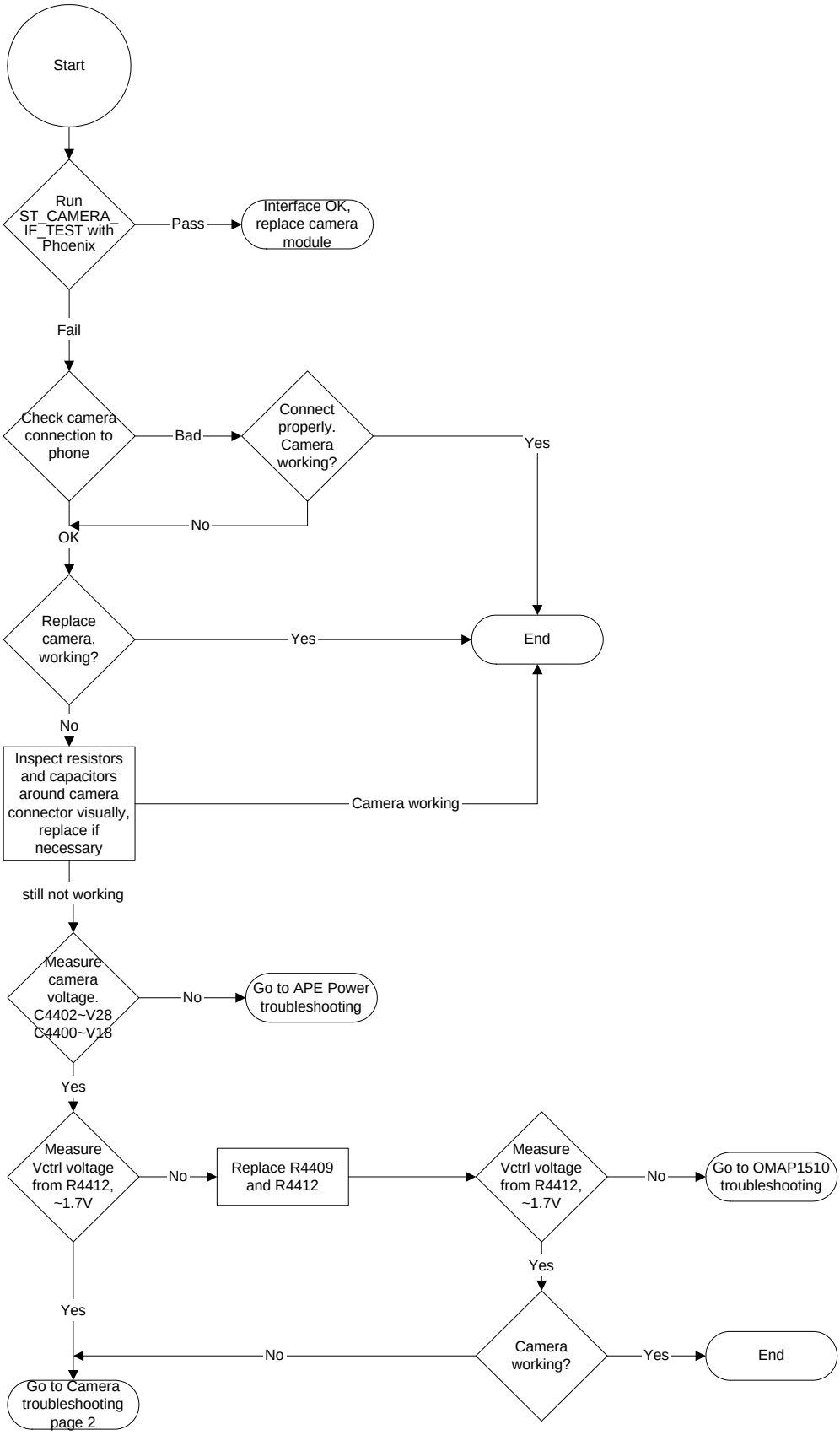
USB troubleshooting

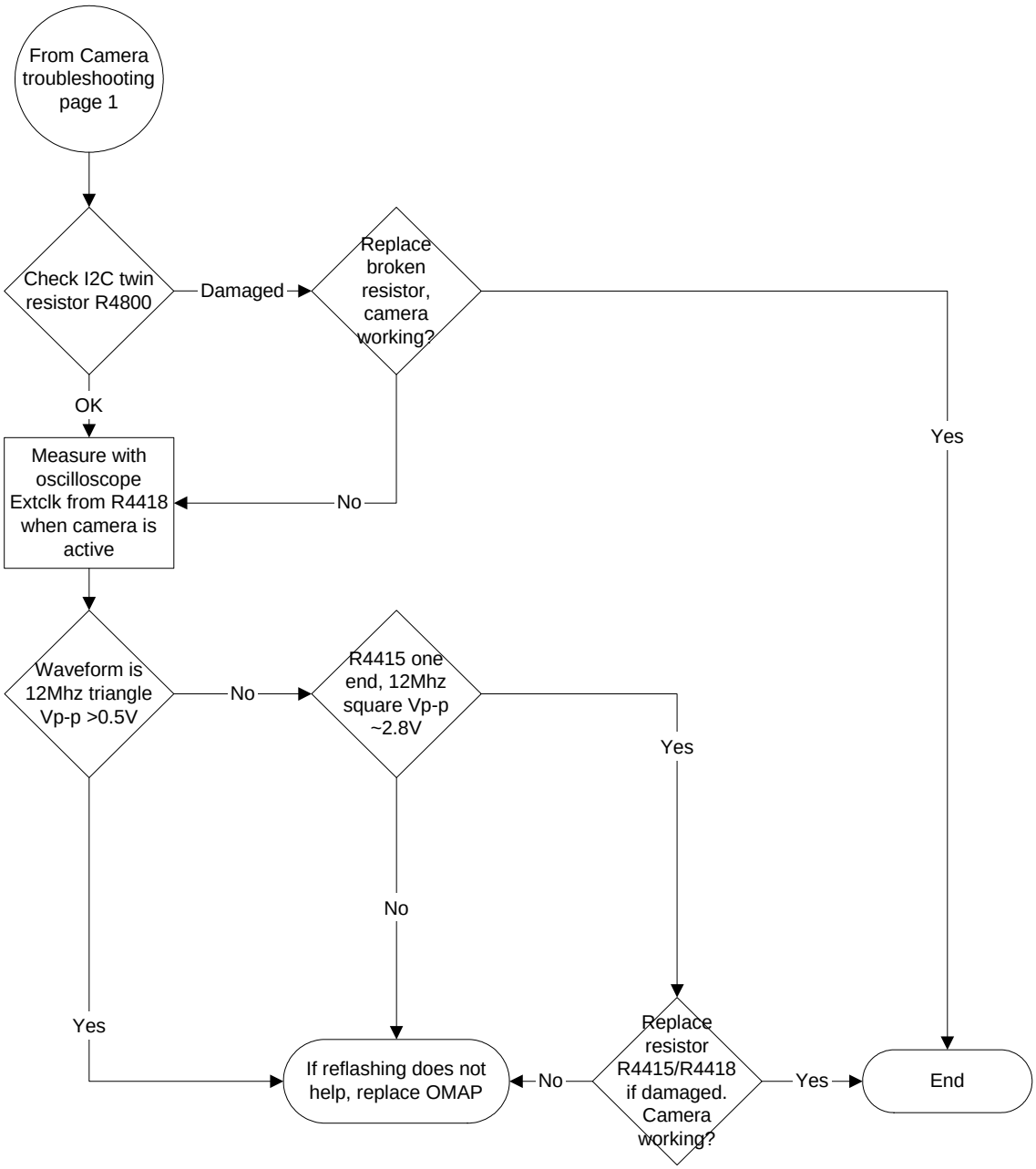


Flash faults



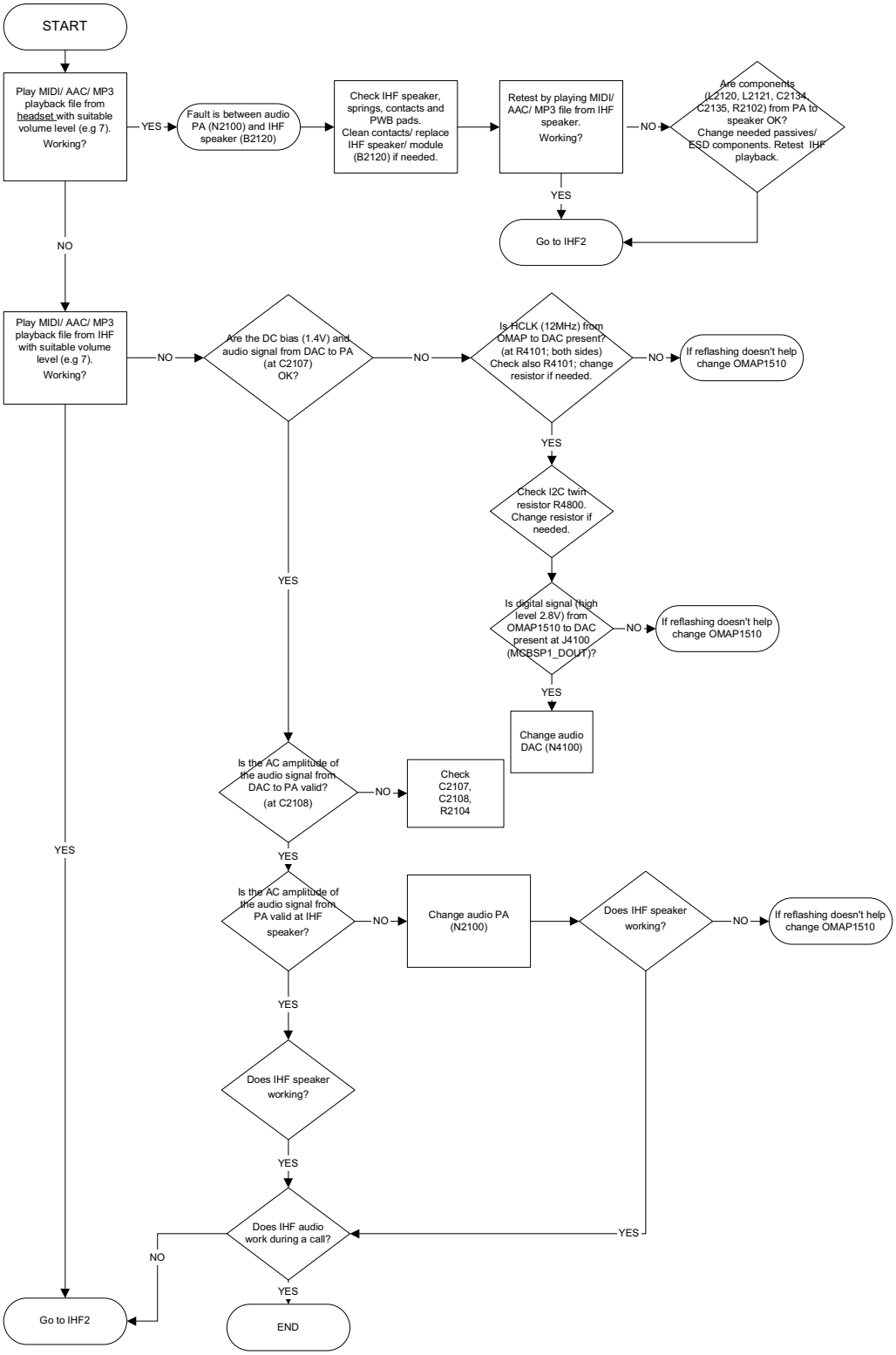
Camera module troubleshooting

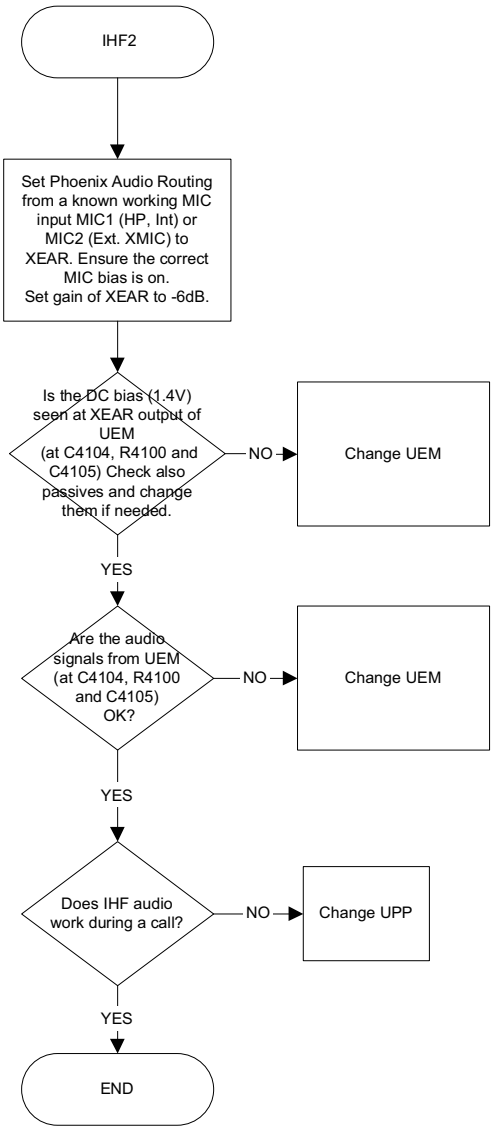




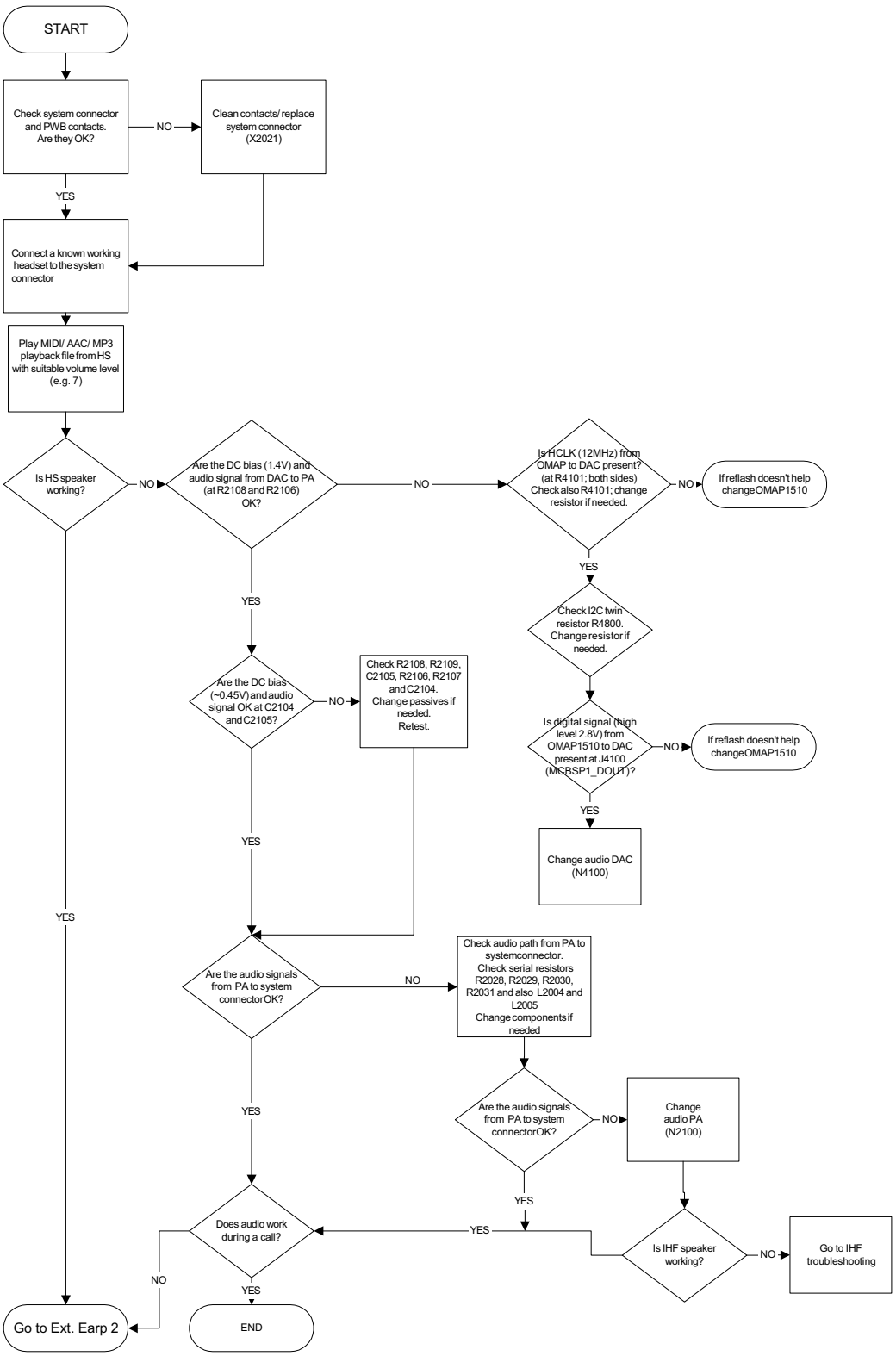
Audio faults troubleshooting

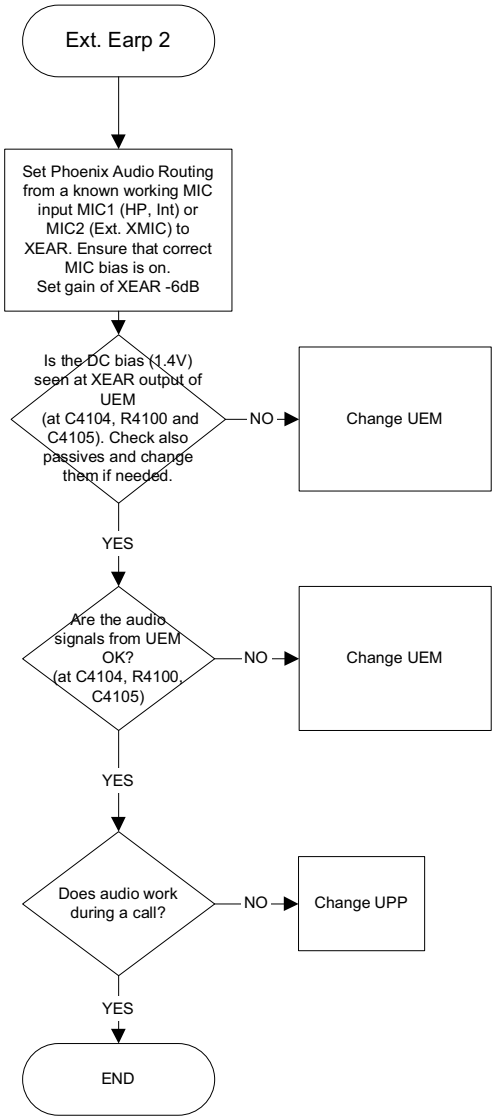
Internal handsfree troubleshooting



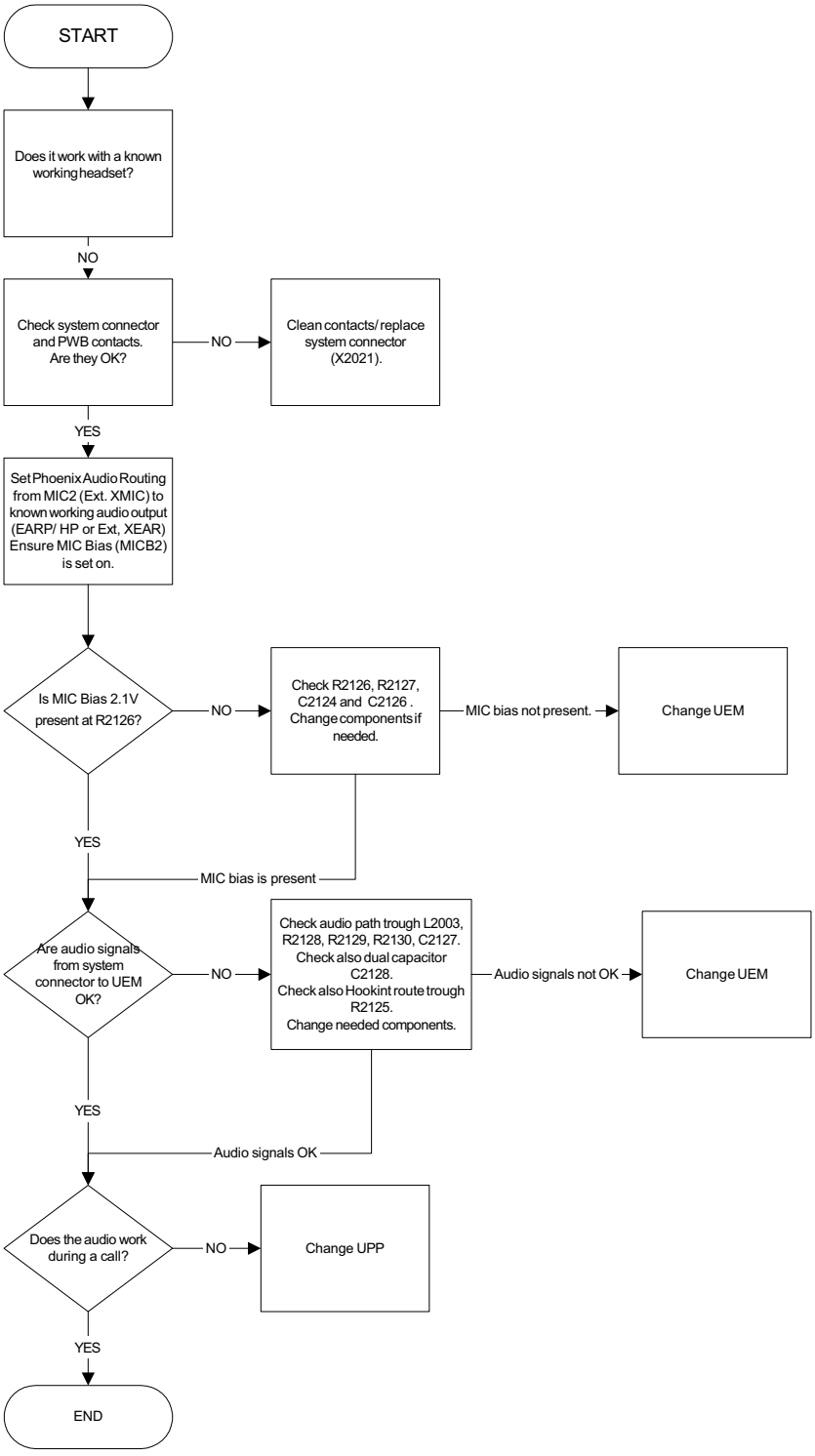


External speaker troubleshooting

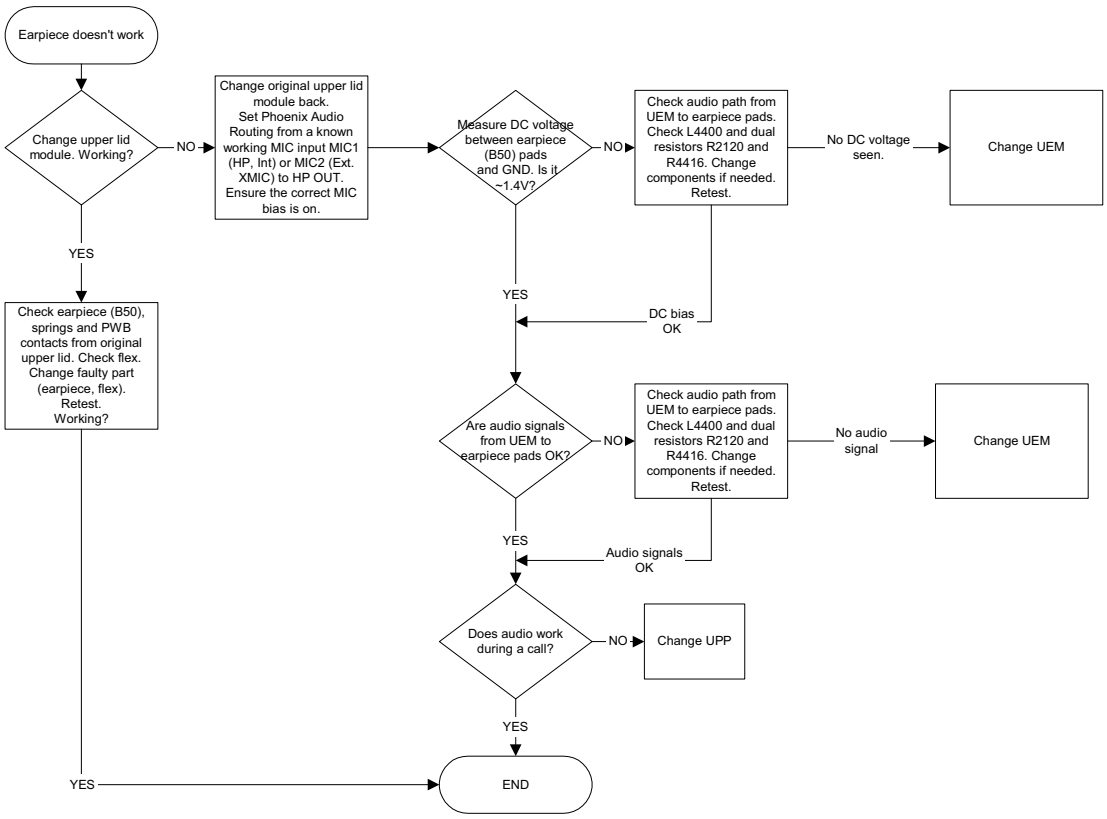




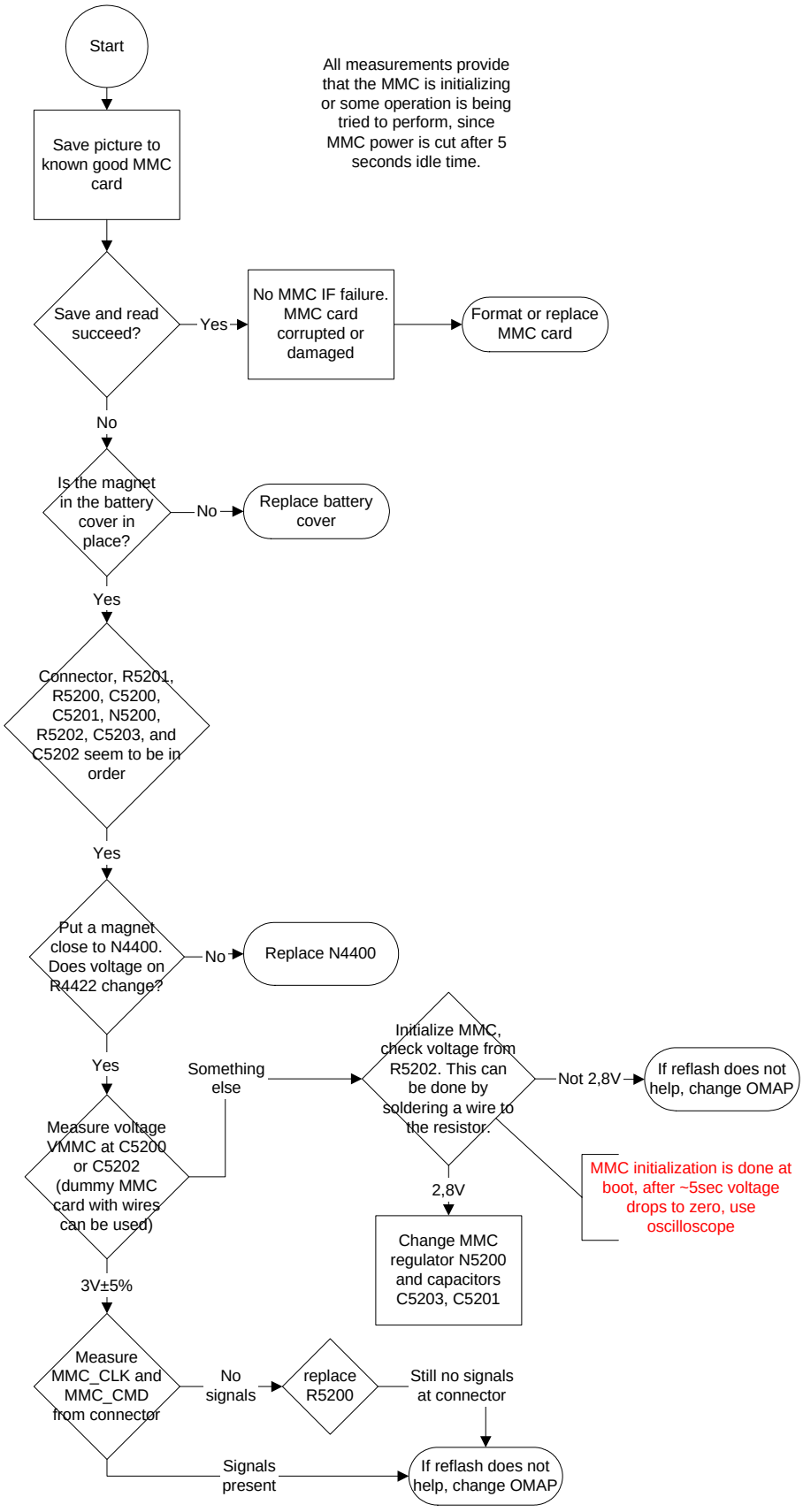
External mic troubleshooting



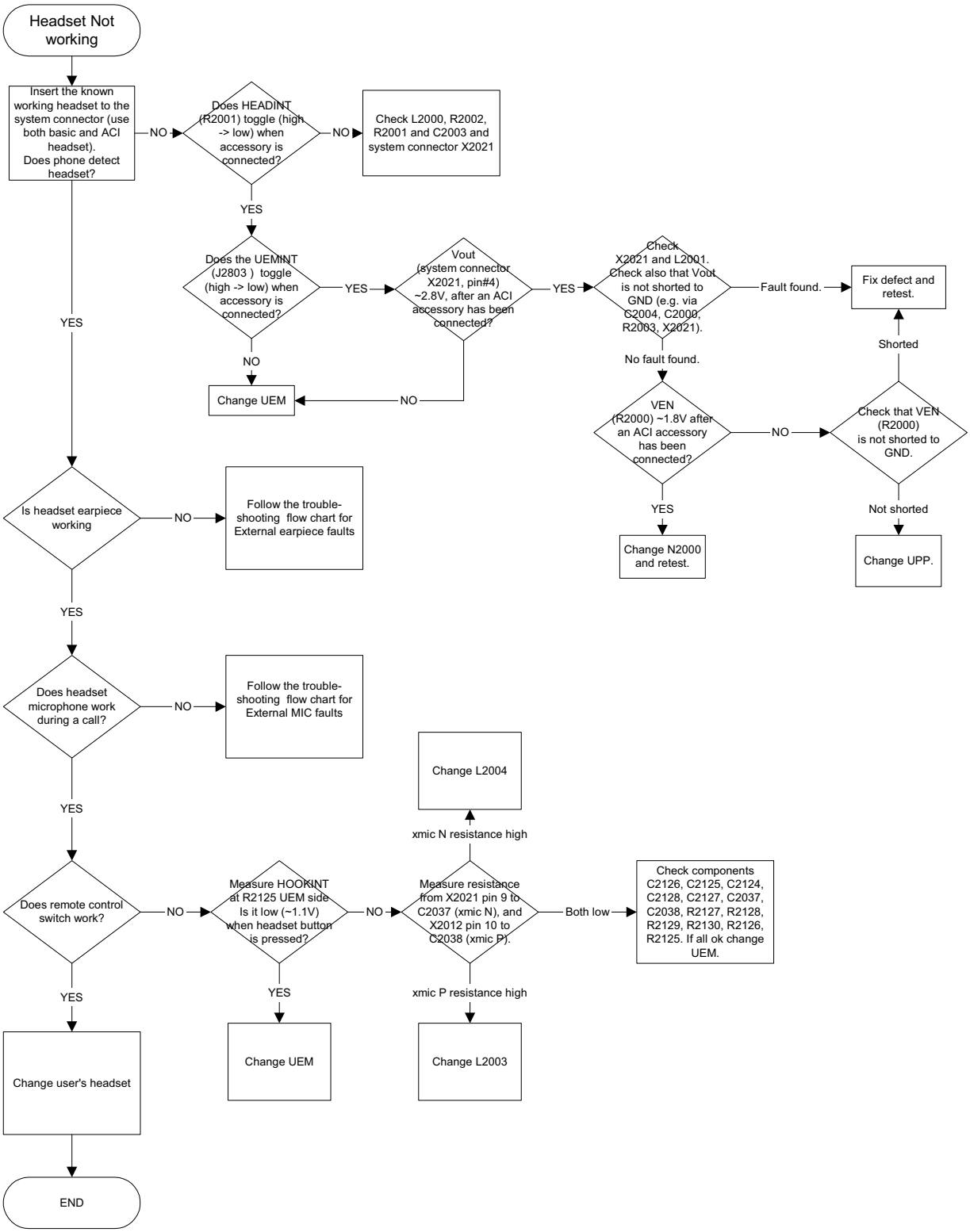
Earpiece troubleshooting



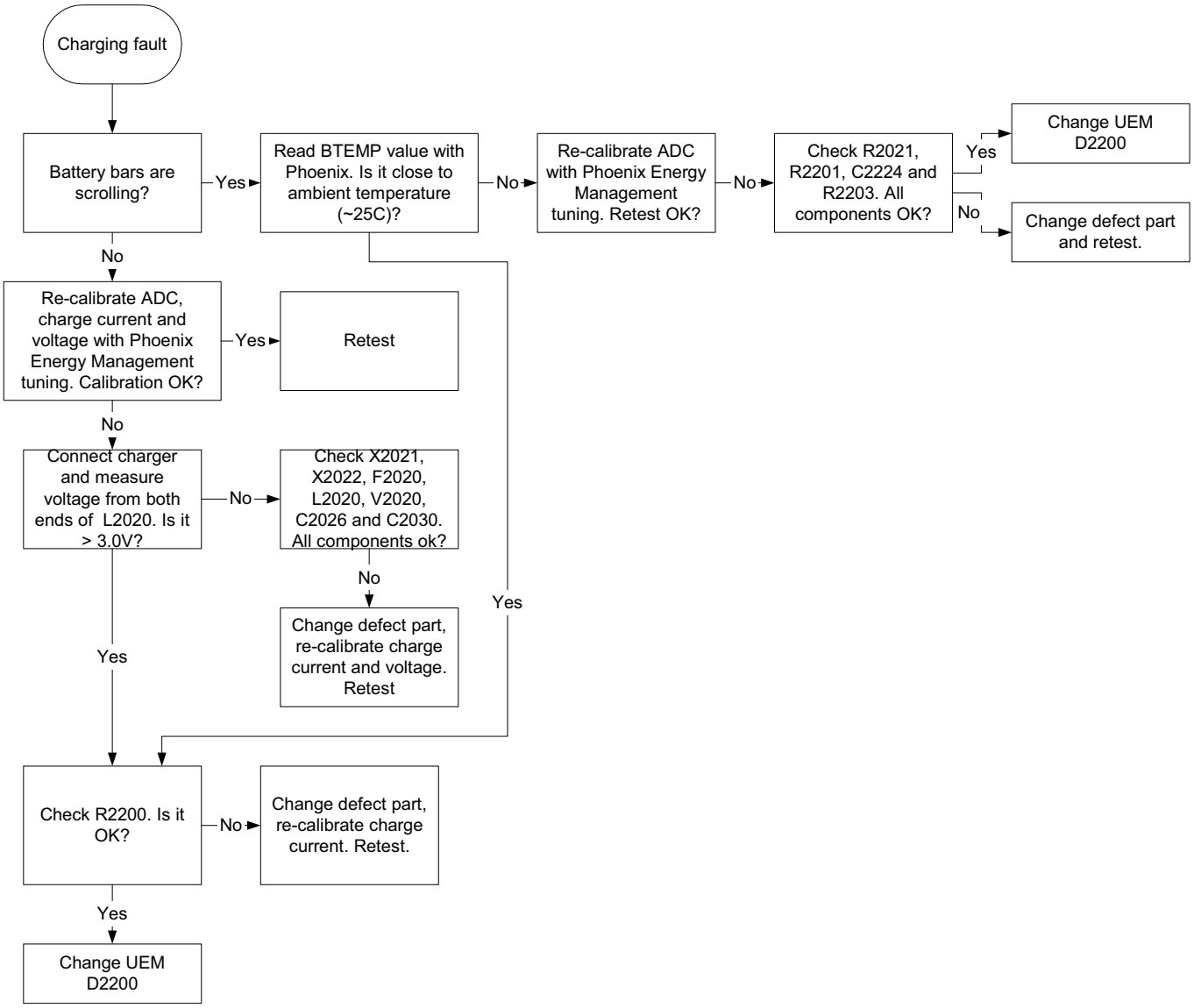
MMC troubleshooting



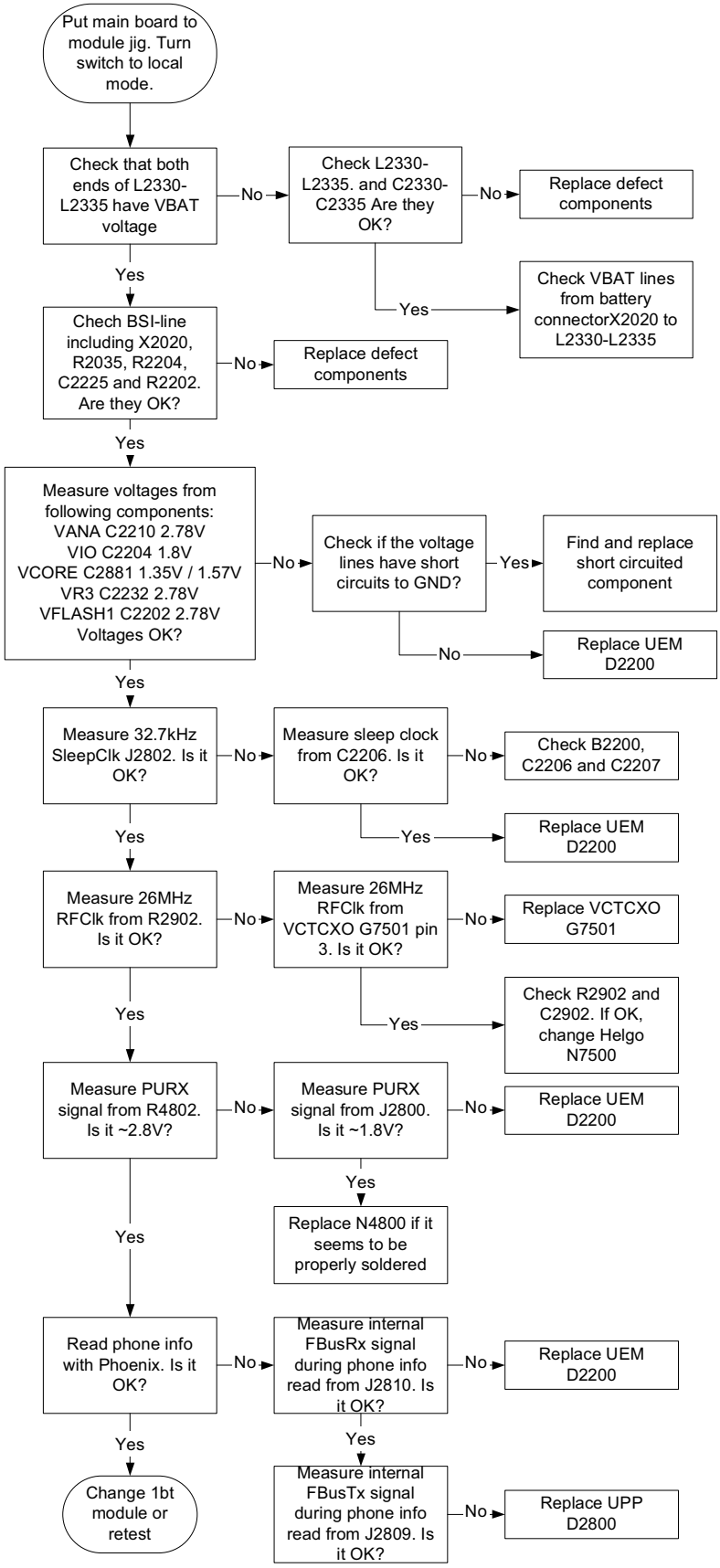
Accessory detection troubleshooting



Charging troubleshooting

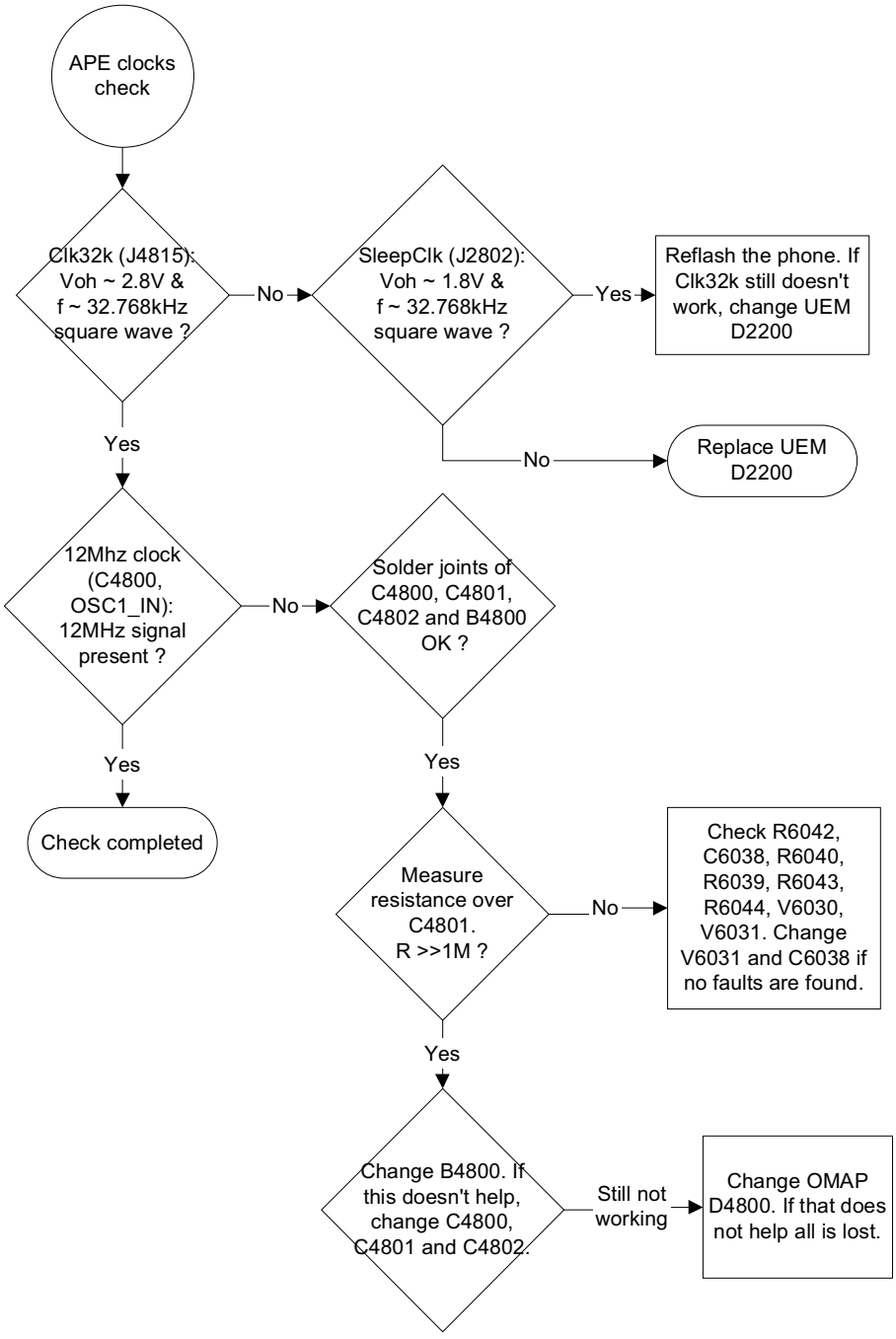


CMT troubleshooting

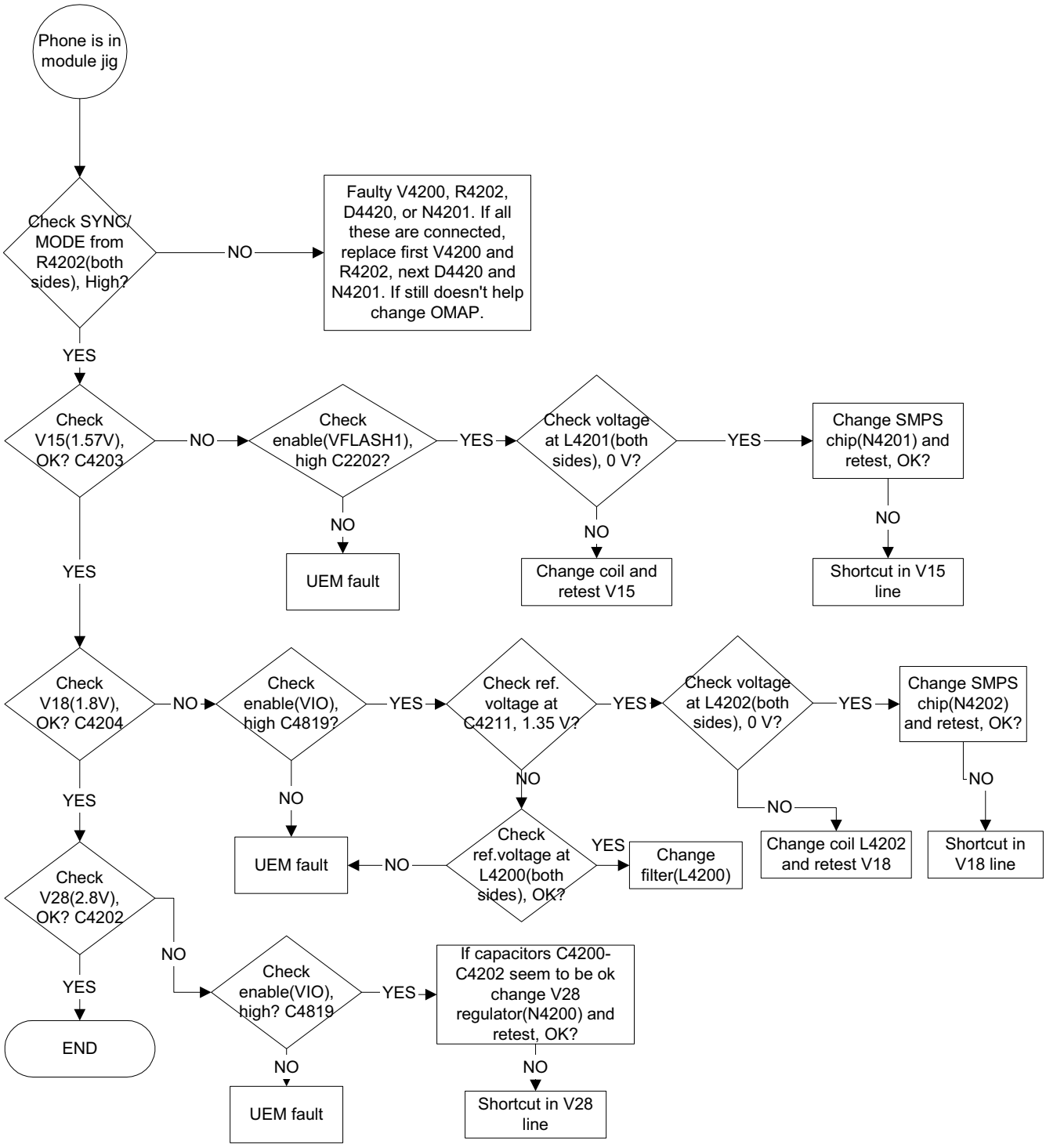


APE troubleshooting

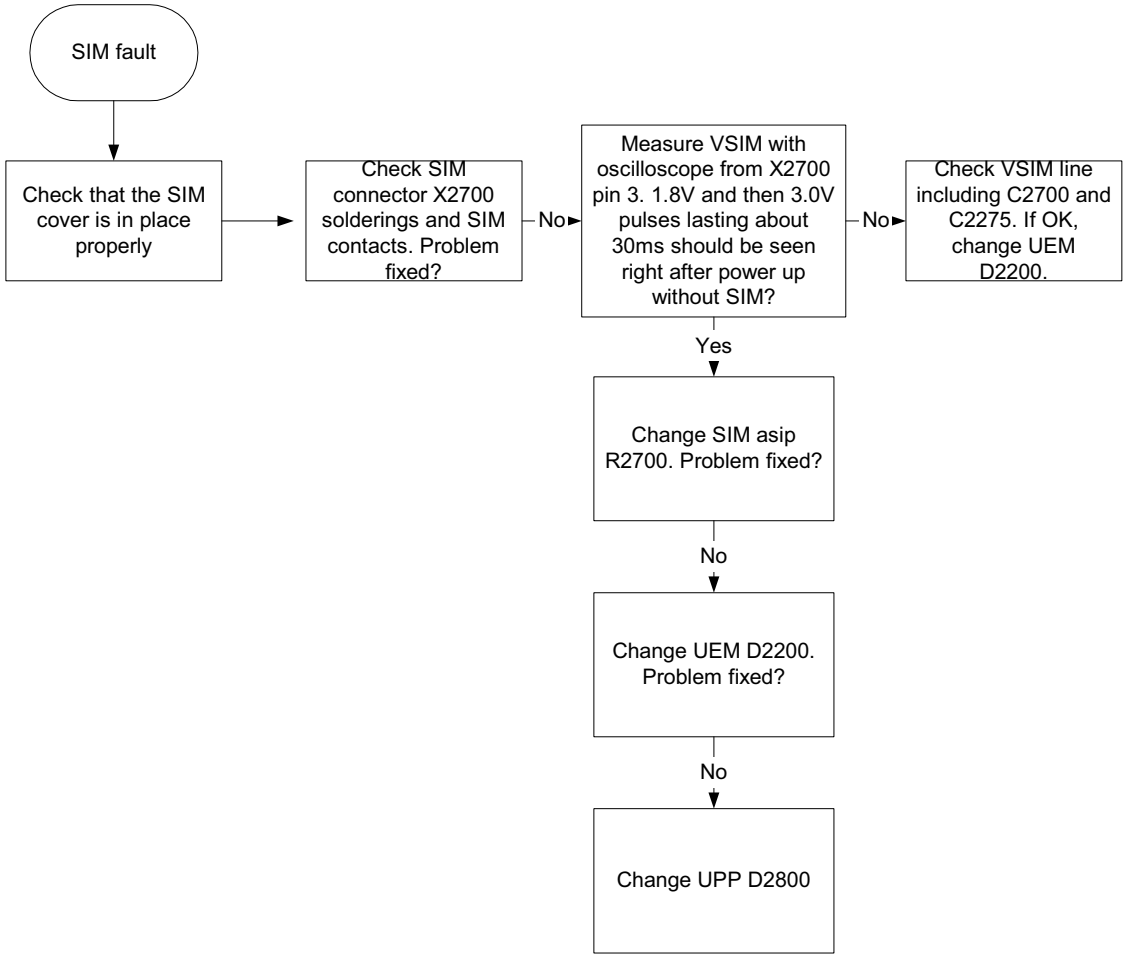
APE clocks troubleshooting



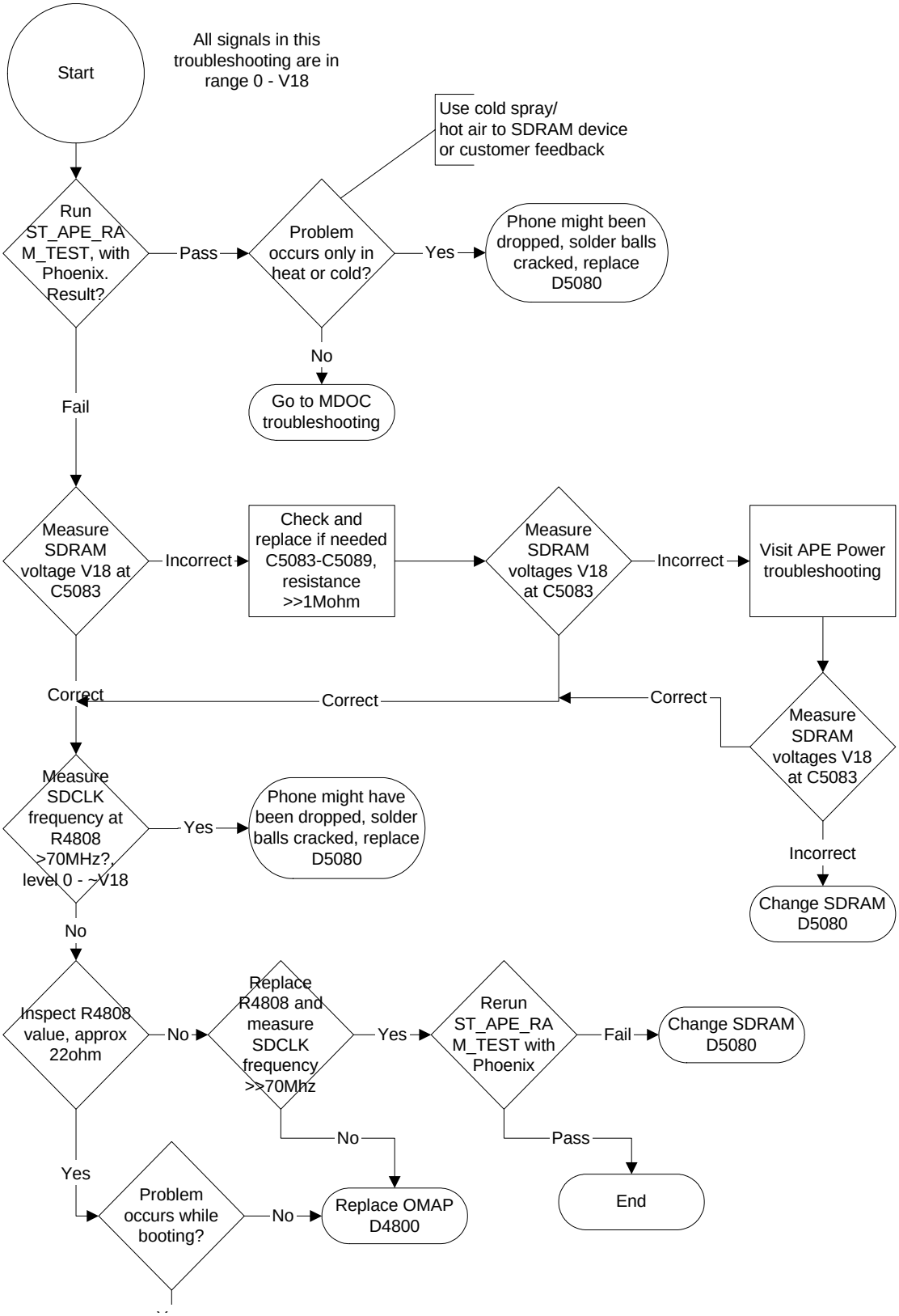
APE energy management troubleshooting



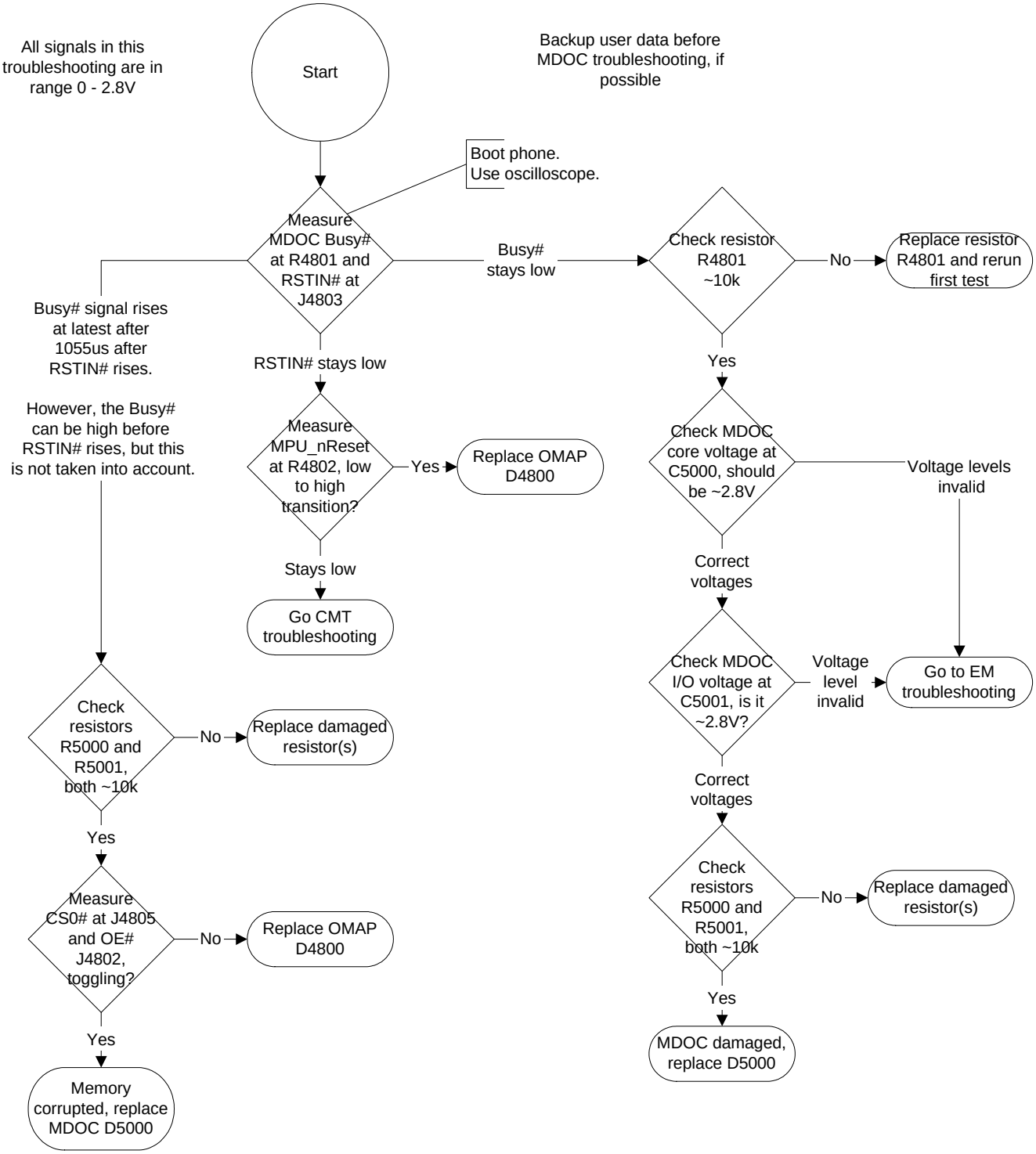
SIM card error



APE memory troubleshooting



MDOC troubleshooting



Appendix A: BB Troubleshooting Measurement Points by Troubleshooting Tree

Table 15: Flash faults

Signal	Voltage	Measurement point
PURX	2.8	J2800
FBUS TX		J2809

Table 16: USB troubleshooting

Signal	Voltage	Measurement point
USB D+	-	X2021 pin 6 to 4 (bottom side)
USB D-	-	X2021 pin 7 to 9 (bottom side)
VBUS	5	C2006
USB enable	2.8	R2004
USB operating voltage	3.3	C2005

Table 17: IR troubleshooting

Signal	Voltage	Measurement point
IR RX	2.8	N4490 pin 4
IR TX	2.8	N4490 pin 3

Table 18: WLAN troubleshooting

Signal	Voltage	Measurement point
V28_WLAN_RF	2.8	C6302
V28_WLAN_RF enable	2.8	N6300 pin 3
V18_WLAN_ANA	1.8	C6307
V18_WLAN_ANA enable	2.8	N6302 pin 3
V28_WLAN_DIG	2.8	C6310
V28_WLAN_DIG enable	2.8	N6303 pin 3
V18_WLAN_DIG	1.8	C6314
V18_WLAN_DIG switch	2.8	V6300 pin 5

Main 22MHz clock	1.8	R6305
EEPROM serial IF	2.8	D6310 pins 5 and 6

Table 19: Bluetooth troubleshooting

Signal	Voltage	Measurement point
Vreg	2.8	C6036
VDD_ANA	1.8	C6031
12MHz clock	~400-900mV	R6043

Table 20: Backlight troubleshooting

Signal	Voltage	Measurement point (all on flex)
LED driver output	10-12	C1151
Regulator enable	1.8	J55
dlight		J56
LED voltage		X1152 pins 2, 3 and 4
PWM		X1150 pin 46
CMT display back-light		X1150 pin 1 and 12
dlight		X1150 pin 45

Table 21: PDA display troubleshooting

Signal	Voltage	Measurement point
Vdd for display	2.8	X50 pin 41
!CS	2.8	X50 pin 3
SCL	2.8	X50 pin 5
DIN	2.8	X50 pin 28
DOUT	2.8	X50 pin 27
!RES	2.8	X50 pin 30
VS	2.8	X50 pin 26
HS	2.8	X50 pin 22
DE	2.8	X50 pin 21
PCLK	2.8	X50 pin 11

PXCL1-16	2.8	X50

Table 22: CMT display troubleshooting

Signal	Voltage	Measurement point (all on flex)
VDD		X50 pin 57
VDDI		X50 pin 58
CSX		J65
SCL		J64
SDA		J63
CSX		J61
SCL		J60
SDA		J59
RESX		J66
RESX		J62

Table 23: Keyboard malfunction troubleshooting

Signal	Voltage	Measurement point
I2C pull-up	2.8	R4800

Table 24: Camera troubleshooting

Signal	Voltage	Measurement point
power	2.8	C4402
power	1.8	C4400
Vctrl	1.7	R4412
ExtClk	>0.5	R4418
clk	2.8	R4415

Table 25: IHF troubleshooting

Signal	Voltage	Measurement point
Audio to PA	1.4	C2107
HCLK		R4101
Control signal	2.8	J4100

Dac-PA		C2108
Audio to speaker		IHF pads
XEAR output	1.4	C4104, R4100, 4105

Table 26: External speaker troubleshooting

Signal	Voltage	Measurement point
Audio dac-PA	1.4	R2106
HCLK		R4101
Audio	0.45	C2104, C2105
Digital audio	2.8	J4100
Audio to pop-port		Pop port (X2021) pins 11-14 (bottom)
Audio to XEAR	1.4	C4104, R4100, C4105

Table 27: External microphone troubleshooting

Signal	Voltage	Measurement point
MIC bias	2.1	R2126
Audio from pop port		Pop port (X2021) pins 9 and 10 (bottom)

Table 28: Earpiece troubleshooting

Signal	Voltage	Measurement point
Bias and audio to earpiece	1.4	B50 (flex), L4400, R2120, R4416

Table 29: MMC troubleshooting

Signal	Voltage	Measurement point (bottom)
Backcover switch		R4422
VMMC	3	C5200
VMMC enable	2.8	R5202
MMC clk	2.8	MMC connector pin 5
MMC cmd	2.8	MMC connector pin 2

Table 30: Accessory detection troubleshooting

Signal	Voltage	Measurement point
headint		R2001 (bottom)
UEMInt		J2803
VOUT	2.8	Pop port (X2021) pin 4 (bottom)
VEN	1.8	R2000
HookInt	1.1	R2125
resistance		X2021 pin 9 to C2037, (bottom) and X2021 pin 10 to C2038 (bottom)

Table 31: CMT troubleshooting

Signal	Voltage	Measurement point
VBAT		L2330 – L2335
VANA	2.78	C2210
VIO	1.8	C2204
VCORE	1.35/1.57	C2881
VR3	2.78	C2232
VFLASH1	2.78	C2202
32kHz sleepclk		J2802, C2206
26MHz RF clk		R2902, G7501 pin 3
PURX	~2.8/1.8	R4802, J2800
FBusRx		J2810
FBusTx		J2809

Table 32: Charging troubleshooting

Signal	Voltage	Measurement point
Charger voltage	>3	L2020 (bottom)

Table 33: APE clocks troubleshooting

Signal	Voltage	Measurement point
32kHz sleep clock	2.8	J4815

32kHz sleep clock	1.8	J2802
12Mhz clock in		C4800
resistance		Over C4801

Table 34: APE energy management troubleshooting

Signal	Voltage	Measurement point
Sync/mode		R4202 (bottom)
V15	1.57	C4203
V15 enable (Vflash1)		C2202
V15 smps		L4201
V18	1.8	C4204
V18, V28 enable (VIO)		C4819
V18 ref voltage	1.35	C4211
V18 smps		L4202
V28	2.8	C4202 (bottom)

Table 35: SIM troubleshooting

Signal	Voltage	Measurement point
VSIM		X2700 pin 3 (bottom)

Table 36: APE memory troubleshooting

Signal	Voltage	Measurement point
SDRAM power	1.8	C5083
resistance		C5083 to C5089
SDRAM clk	1.8	R4808
resistance		Over R4808

Table 37: MDOC troubleshooting

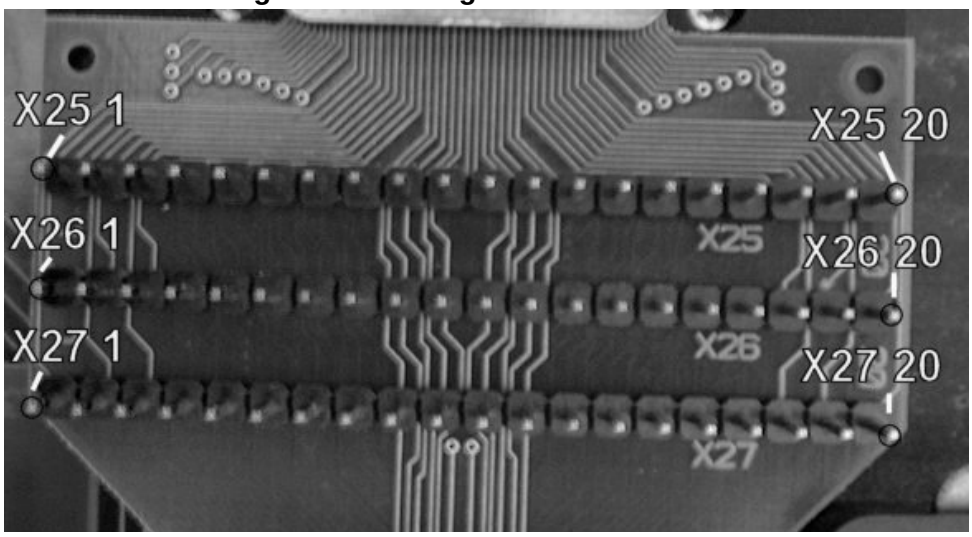
Signal	Voltage	Measurement point
Busy		R4801
RSTIN		J4803

resistance		R4801
MDOC core voltage	2.8	C5000
resistance		of R5000 and R5001
MDOC IO voltage	2.8	C5001
CS0		J4805
OE		J4802

Table 38: Flex signal test connector pin arrangement

Pin	X25	X26	X27
1	LCD_PXL3	LCD_PXL4	GND
2	LCD_PXL0	LCD_PXL1	LCD_PXL2
3	LCD_PXL8	LCD_PXL9	LCD_PXL10
4	WIRE_SDO	WIRE_nSCS3	GPIO13
5	GND	LCD_VSYNC	WIRE_SDI
6	LCD_HSYNC	GND	GND
7	LCD_PXL5	LCD_PXL6	LCD_AC
8	GND	GND	LCD_PXL15
9	KBR4	V28	LCD_PXL7
10	KLIGHT	KBC0	WIRE_SCLK
11	DLIGHT	CALLED 1	VBAT
12	KBR3	KBR2	PWRONX
13	LCD_PXL14	LCD_PXL13	LCD_PXL12
14	LCD_PXL11	LCD_PCLK	KBC1
15	GND	GND	GND
16	GND	KBC2	KBC3
17	KBC4	KBC5	WIRE_nSCS0
18	KBR0	GPIO12	EARP
19	EARN	KBR1	V18
20	V28	GND	GND

Figure 20:Flex signal test connector



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